Control Methods for Multilevel Converters

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ABSTRACT

This thesis aims to develop new control methodologies for the Packed U-Cell (PUC) converter. The main problem lies in the structure of the PUC converter, where it is a hybrid type of multilevel converter (MLC) similar to cascaded H-bridge converters. From the control prospective, the topology has discrete digital control inputs, thus conventional modulation techniques cannot be directly applied to the converter. Proper control methods have to be introduced in order to make use of the great advantages of the PUC converter. These control methods have to be simple in implementation for industrial environment with low switching frequency. Additionally, the newly proposed control methods should have advantages over the existing ones.

In the first attempt of this thesis, a modified version of model predictive control (MPC) has been integrated to control grid connected PUC inverters. Mainly, the cost function is formulated to guarantee the stability of the controlled system. Then, the gains associated with the controlled variables are eliminated in order to simplify the control. The proposed controller has shown great features in terms of stability and low average switching frequency.

In the second attempt of this thesis, the interesting features of sliding mode theory are utilized to serve the control problem in a better way. The proposed controller is very simple to implement with low computation time, which reduces the computational burden on the controller. The controller aims to allocate the control input which stabilizes both the grid current and the auxiliary capacitor voltage in the grid

connected PUC inverter.

Lastly, the control problem of the PUC rectifier with a dual output is targeted using Lyapunov-based MPC. This attempt is done in order to prove the workability of the controller for three control variables. In this method Lyapunov-based MPC doesn't require gain tuning as in the PUC inverter problem. Load current measurements are eliminated by making use of the mathematical model of the PUC converter. This significantly reduces the cost and simplifies the control algorithm, where no current sensors are used for the load measurements.

For all proposed methods, simulations and experimental tests were done in order to justify the correctness of the proposed methods. Dynamic tests and parameter mismatch tests are carried out to measure the controller response and to show the robustness feature of the proposed controllers.

Keywords: Finite control set, Lyapunov control, model predictive control, multilevel converter, packed U-Cell converter, sliding mode control.

ÖZ

Bu tezin amacı PUC çevirgeçler için yeni denetleme yöntemleri geliştirmektir. Bu çevirgeçlerde esas sorun, ardarda bağlanmış H-köprüye benzer çoklu-seviyeli melez bir sınıf olmalarından kaynaklanan yapılarından dolayıdır. Denetleme açısından bakıldığında, bu çevirgeçlerin topolojisinde ayrık ve sayısal denetleme girişleri vardır. Dolayısıyla, geleneksel kipleme yöntemleri bu çevirgeçlere doğrudan uygulanamaz. PUC çevirgeçlerinin avantajlarından faydalanan uygun denetleme yöntemlerinin geliştirilmesi gerekir. Bu yöntemlerin, endüstriyel ortamlara uygun ve düşük anahtarlama sıklıklarına sahip basit bir şekilde gerçekleştirilebilmeleri gerekir. Buna ek olarak, önerilen denetleme yöntemlerinin var olanlara göre avantajlarının olması gerekir. Model öngörücü denetlemenin (MÖD) çoklu-seviyeli çevirgeçler gibi endüstriyel uygulamalarda kullanılması da dikkate alınarak, bu yöntemin farklılaştırılmış bir türü şebekeye bağlı PUC evirgeçlerinin denetlenmesi için geliştirilmiştir. Esas olarak eder işlevi, denetlenen sistemin kararlılığını garanti edecek şekilde düzenlenmiştir. Denetlenen değişkenlere ait kazançlar, bazı varsayımlar kullanılarak ve denetlemeyi basitleştirmek amacı ile elenmiştir. Önerilen denetleyicinin, kararlılık ve düşük ortalama anahtarlama sıklığı gibi önemli özelliklere sahip olduğu gözlenmiştir.

Bu tezdeki ikinci girişimde, denetleme sorununa daha iyi çözümler getirmek için, kayan kiplemeli denetleme kuramının önemli özelliklerinden yararlanılmıştır. Önerilen denetleyici, denetleyicinin üzerindeki hesaplama yükünü azaltan, oldukça basit bir tarzda gerçekleştirilebilmektedir. Denetleyicinin amacı denetleme girişlerini, şebekeye bağlı PUC evirgeçinin şebekeye verdiği akımı ve sığaç gerilimini kararlı

duruma getirecek şekilde belirlemektir.

Son olarak, çift çıkışlı PUC doğrultucuların denetleme sorununu Lyapunov tabanlı MÖD kullanarak çözmek hedeflendi. Bu girişim, üç değişkenli denetleme durumunda denetleyicinin çalışabilir olduğunu göstermek için yapıldı. Önerilen yöntemde, PUC evirgeçinde olduğu gibi, Lyapunov tabanlı MÖD kazanç ayarına gereksinim duymamaktadır. PUC çevirgeçinin matematiksel modeli kullanılarak yük akımı ölçümleri elenmiştir. Bu da, denetleme algoritmasını basitleştirmiş ve akım duyaçlarına gereksinimi ortadan kaldırarak ederi önemli ölçüde azaltmıştır.

Önerilen ve PUC topolojisine uygulanan denetleme yönteminin başarımını göstermek amacıyla benzetim ve deney sonuçları sunulmuştur. Denetleyicinin yanıt hızını ölçmek ve sağlamlık özelliğin göstermek amacı ile dinamik ve parametre uyuşmazlığı sınamaları yapılmıştır.

Anahtar Kelimeler: Sınırlı denetim kümesi, model öngörülü denetim, çok katmanlı çevirgeç, istiflenmiş U-hücre çevirgeç, kayan kipli denetim.

DEDICATION

Dedicated to my family.

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After all, I believe that the research I did during my PhD is just an exercise and the best is coming with time. This is just the beginning.

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LIST OF SYMBOLS AND ABBREVIATIONS

CHB	Cascaded H-Bridge
FCC	Flying Capacitors Converters
FCS-MPC	Finite Control Set Model Predictive Control
FCS-SMC	Finite Control Set Sliding Mode Control
MLC	Multilevel Converter
MLI	Multilevel Inverter
MPC	Model Predictive Control
NPC	Neutral Point Clamped
PI	Proportional Integral
PLL	Phase-Locked-Loop
PUC	Packed U-Cell
PUC5	5-Level Packed U-Cell
PUC7	7-Level Packed U-Cell
SM	Sliding Mode
SMC	Sliding Mode Controller
THD	Total Harmonic Distortion

Chapter 1

INTRODUCTION

1.1 Introduction

With the rapid proliferation of renewable energy systems, the need for efficient and high-performance power conversion capabilities has become vital. A Multilevel Converter (MLC) is one among many recent technologies to address this issue. Nowadays, MLC has become a mature technology which is thriving hastily with the growth of renewable energy usage. The limited voltage blocking capability of the power switches is the major reason behind the development of multilevel converters. Though this capability has been improved with the improvement of production technologies, the reachable voltage is still lower than the service voltage of high voltage equipment. Moreover, multilevel converters are key factors in improving the power quality in power conversion systems [2].

Researchers in the field of industrial power electronics are making considerable efforts to improve energy efficiency, power density, reliability, and reduce overall cost of MLCs. The advantage behind using MLCs includes the possibility to use low voltage-rated switches, achieving low-distortion output current waveform, reducing the switching events as well as the size of output filters. The structure of MLCs allows their employment with renewable energy sources and battery systems. The redundant states in MLCs, which may occur naturally, make it possible to achieve

fault tolerant operation [3, 4].

1.2 Thesis Objectives

As the packed U-Cell (PUC) converter is introduced as a high density power solution in industrial applications, this indeed has side effects on the performance of the converter. Indeed, specially designed controllers are required for this compact form of converter. In this section, the main objectives of the thesis are listed to overcome the difficulties in the controller design of the PUC. Firstly, when the PUC is introduced for grid connected inverter applications, we have two main concerns regarding controller design: 1) gain tuning; 2) simplicity of design. These concerns lead to think of a new design procedure in order to achieve the required goals. Thus, Lyapunov-based model predictive control is presented in Chapter 3 as a solution to overcome the existing problems in conventional model predictive controller.

Furthermore, it is crucial to have a computationally simple and easy-to-implement algorithm which doesn't require excessive processing time and memory. Additionally we need to further reduce the switching frequency of the PUC inverter. This is possible by introducing an allowable error in the auxiliary capacitor voltage to the benefit of reducing the average switching frequency. These objective were attainable as presented in Chapter 4. The solution derived based on sliding mode theory, where each of the error variable was designed into a separate sliding function.

Lastly, Lyapunov-based model predictive control is applied to the PUC7 rectifier. The main objectives (in addition to the advantages gained from the Lyapunov-based model predictive control) is to reduce the number of sensors used in the real implementation. This was possible by estimating the load currents from the mathematical model of the converter. The control problem solution is presented in Chapter 5.

1.3 Literature Survey

Classical MLCs in both literature and industry include: Neutral Point Clamped (NPC) [5–8], Flying Capacitor (FCC) [9–11], and Cascaded H-Bridge (CHB) [12–14] Converters. Recently, there have been a lot of interesting research on multilevel converters using nonlinear control methods [15–19], while other research use predictive control and also model predictive control [20–22].

The PUC topology is a MLC, which was originally proposed by Ounejjar et al. [23–27]. Besides its simple construction, the PUC converter has the advantage of reduced number of switches and DC sources as compared to other classical MLC topologies. Moreover, the reduced number of switches implies a reduced number of redundant states, which adds challenges to the control design [1, 23, 25, 26, 28–35]. The PUC topology has been tested in several applications such as three-phase active filters [36], static VAR compensators [37, 38], dynamic voltage restorers [39] and other industrial applications [40–47].

In [29], authors have proposed a novel six band hysteresis controller for the converter operating in inverter and rectifier mode. In rectifier mode for instance, the error of the two output load voltages are regulated by means of a PI controller, then by using a hysteresis controller the rectifier line current is controlled. It was clearly shown that the controller has fast dynamic, strong robust behavior and simplicity in implementation, but it still suffers from variable switching frequency. On the other hand, a fixed switching frequency could be maintained when PID controllers are used, with the integration of the PWM technique, as reported in [26, 28]. In [46] capacitor voltage balancing was possible by means of choosing a proper firing angle of the switches, which was extensively addressed in [48] for generalized multilevel

inverters.

Model predictive control (MPC) is used in plants which have complex dynamics and can flexibly handle non-linearities as well as constraints on variables. In such plants, the dynamic model of the controlled plant is used to produce the optimal control input at the current time instant [49]. The "optimal" choice is determined by solving an optimization problem according to some error cost function, which is evaluated based on the measured states, the previous states and the predicted ones. The predicted states require estimation which is obtained based on the mathematical model of the plant, and the control action is taken over one finite horizon (longer horizons are also possible). The control input may be continuous in time, taking values in a certain range, or it may consist of a finite set of discrete inputs.

The nature of the control input emerges from the controlled system's structure. Therefore MPC when applied to finite control set problems has a variable switching frequency output and the optimization problem is solved by evaluating an online cost function for all the possible control inputs. In continuous input MPC problems, the controller requires a modulator, resulting in fixed switching frequency and the optimization problem may be solved offline. For both types of MPC problems, constraints may be included in the controller in order to further improve the performance of the controlled system [50]. This feature is considered as another great advantage of model predictive-based controllers especially when the model includes nonlinearities [51].

With the existing fast digital controllers, MPC offers intuitive solutions for power-electronics-related control problems along with a remarkable ease of implementation,

efficient and satisfactory performance [32, 52, 53]. MPC can solve multi-objective control problems such as the control of the PUC inverter [1,39,54,55]. By using MPC, an optimal sequence of the control signals is obtained over the prediction horizon by the minimization of a multi-objective cost function (simultaneous control of the grid current and the capacitor voltage). Then, the first switching pattern of the control sequence is conveyed to the inverter switches and the entire "prediction-optimization" operation is repeated at each sampling period [1,56]. For inverter applications, in [54] the cost function was defined in terms of the load current as well as capacitor voltage errors, coupled with weighting factors to be selected such that minimum total harmonic distortion (THD) of the grid current, and low capacitor voltage error are obtained.

However, the main drawbacks of the MPC techniques are the involvement of considerable time intervals between the control actions (computation time) to allow the minimization of the cost function, complex tuning of the control gains (weighting factors), and high switching frequency [57–61]. Thus, sliding mode control may offer a simple and effective alternative for the PUC control problem. Sliding mode control is a particularly interesting technique [62–68] where the principle consists in bringing, regardless of the initial conditions, the representative point of the system behavior along a cross-surface (sliding surface) by the application of switching elements in the control law. In addition, the set-valued control ensures that the system representative state reaches the sliding surface in a finite time and the system starts moving toward the steady state. The sliding surface is designed as a linear combination of the system states, which usually represent system errors. The control technique then becomes insensitive to disturbances and parametric variations, which makes it a good candidate for the PUC converter under study.

1.4 Contribution of the Thesis

The main contribution of this thesis is the ability to soften the existing nonlinear control methods in order to overcome the difficulties in the PUC converter. The well-known Lyapunov control theory is adapted to serve the existing model predictive control method in order to overcome the structure of the PUC topology and to improve the performance of the model predictive controller. The reported Lyapunov based predictive control is a novel method which will solve the existing limitations in the model predictive control, such as gain tuning, inclusion of additional constraints and simplicity in implementation. On the other hand, the existing sliding mode control theory is set in a simple form which yielded a great reduction in the processing time and further simplicity in the implementation. The reported sliding mode control is model independent type of control, where the control algorithm has the merit of reducing the average switching frequency at the expense of allowable error in the capacitor voltage. Additionally, the presented control methods are not restricted to this topology but can be directly applied to other topologies as well. In this thesis each chapter is dedicated to a novel control technique applied to multilevel Packed U-Cell converters.

In Chapter 3 a new Lyapunov-based model predictive controller is proposed for a 7-Level Packed U-Cell (PUC7) grid-connected inverter. The cost function of the proposed model predictive controller is designed from a system stability point of view, inspired by Lyapunov control theory. The proposed controller eliminates the need for gains that are used to penalize errors on controlled system variables associated with cost function coefficients, as seen in classical MPC-based controllers. Therefore, the control design problem is significantly simplified. In addition, the

average switching frequency is also reduced, as shown in both simulation and experimental results, leading to a reduction in switching losses. Simulation and experimental tests on a PUC7 lab prototype, demonstrate the excellent performance of the proposed control system, in terms of high disturbance rejection, robustness to parameter mismatches, and fast dynamic response. Such features qualify the proposed control strategy as a good candidate for grid-tied applications.

Chapter 4 proposes an effective sliding mode controller (SMC) for a grid-connected PUC7 inverter. The aim is to design a simple controller that deals effectively with the complex control problem of the PUC7 inverter (multi-objective control problem). The selection of the control actions is achieved according to the system state error at every sampling time regardless of the previous values, which makes the control technique model- independent. The control algorithm evaluates online two cost functions (one for each state error) which are derived based on sliding mode (SM) theory, and selects the optimal control input in order to satisfy the reaching conditions of the two cost functions. Compared to the existing solutions, the proposed SMC technique ensures lower average switching frequency by tuning the hysteresis bandwidth of the capacitor voltage error. The fast implementation, needless of gain tuning, and simple design procedure are the main features of the proposed algorithm. Simulation and experimental results are presented to prove the effectiveness of the proposed technique in controlling the PUC7 inverter with high dynamic performance and robustness against disturbances and parameters mismatch.

Chapter 5 proposes a Lyapunov-based model predictive controller design for dual output multilevel PUC7 rectifier. The proposed controller is seen as an improvement of the conventional model predictive controller, where the cost function is derived

from a stability point-of-view. The controller selects the control input which corresponds to the minimum value of the Lyapunov cost function. Though the cost function includes three state variables' errors (two capacitor voltages and source current errors), the proposed controller is characterized by its easy implementation, no gain tuning requirement as for conventional MPC, and less sensors demand (the controller predicts the loads measurement based on the mathematical model of the PUC rectifier).

1.5 Conclusion

It is evident that the development of the multilevel converter is ongoing and a rapidly growing technology with applications in the electrical power industry. As the need increases for high density power converters, topology designers are looking for more compact form of the device, which leads to topological complexity of the power converter. The compact form reduces the number of passive elements used and semiconductor devices; yet it complicates the control design procedure. This thesis presents competitive solutions to the existing ones in the field of control of PUC power converters. The solutions presented here are aimed to be simple, effective and are based on a mathematical foundation where further studies can be conducted on them. Furthermore, the presented control methods can be easily applied to other types of converters such as cascaded h-bridge and flying capacitors.

Chapter 2

PACKED U-CELL TOPOLOGY

2.1 The Need for MLC

During the last decades, many multilevel topologies were discussed in the literature, which have found their way to industrial applications [69, 70]. There are numerous review and tutorial papers which classify and summarize recent developments in topologies and control methods of MLCs [3, 71–74]. In 1981, Nabae has invented a new type of multilevel converter known as the neutral point clamped (NPC) inverter [75]. In 1992, Meynard et. al. developed the flying capacitor (FCC) type of multilevel converter [76]. After a few years, F. Peng et al. developed the cascaded H-bridge multilevel converter (CHB) for static var generation, which is used for different applications afterwards [77]. The aforementioned three types of converters are known as traditional multilevel converters which have limitations when the number of output voltage levels is increased.

The need for multilevel converters is due the following reasons:

1. In order to reduce the harmonic contents in the output waveform and to reduce the voltage stress across the semiconductor switches.

2. The ability to generate high voltages by employing lower rated devices which have limited blocking capabilities.

3. To reduce the switching frequency (i.e. switching losses).

4. To reduce the filter size and the overall cost.

In the following, the flying-capacitor converter, the cascaded H-bridge converter and then the Packed U-cell topology are presented. A comparison between the PUC and the traditional types of multilevel converter is given.

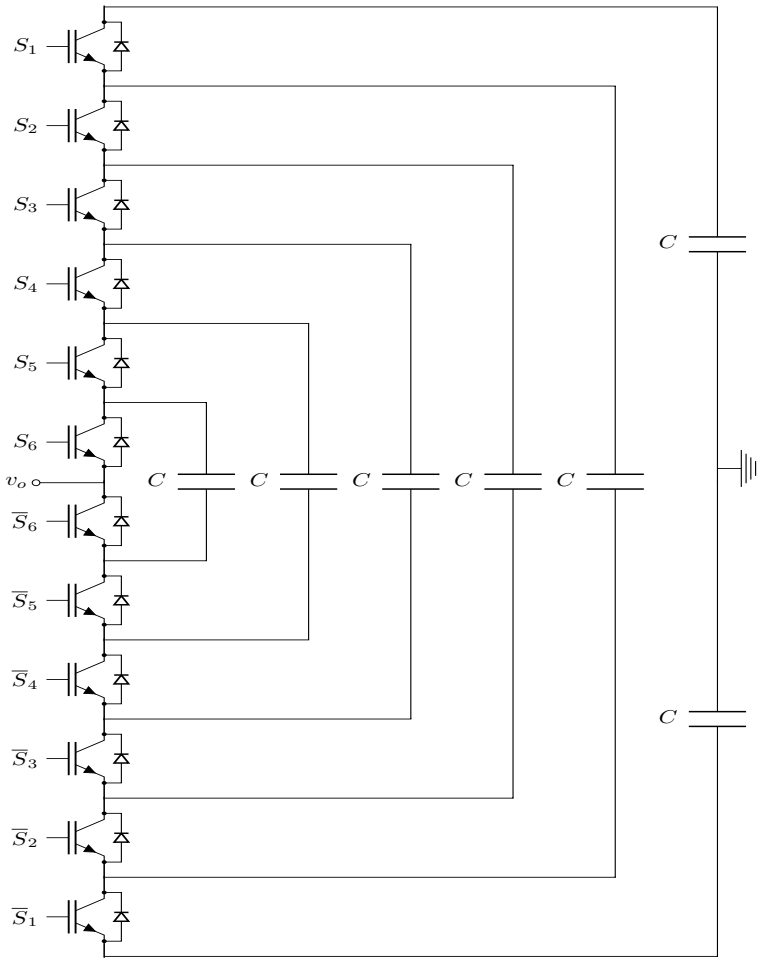


Figure 2.1: Flying capacitors converter topology generates up to 7 levels output waveform.

2.2 Flying Capacitor Converter (FCC)

The word "flying" is used because the capacitor's voltage is floating with respect to the ground and the capacitors are used to "clamp" the voltage to higher/lower levels than the dc source(s) [78–80]. Theoretically, FCC can produce an infinite number of output voltage levels but most of the applications were limited to 5, 7 and 9 level output due to the complexity in the control, gate driver design and capacitor voltage balancing

issues [81, 82]. Figure. 2.1 shows a seven level FCC; the capacitor closer to the dc voltage source has higher voltage stress, while the outermost capacitors have lower voltage stresses and lower switching frequency, as well.

FCC consists of multiple cells nested in each other where each cell has a single capacitor and two power switches. A converter having N cells uses N capacitors and 2N switches to produce N+1 different output voltage levels including the zero output level.

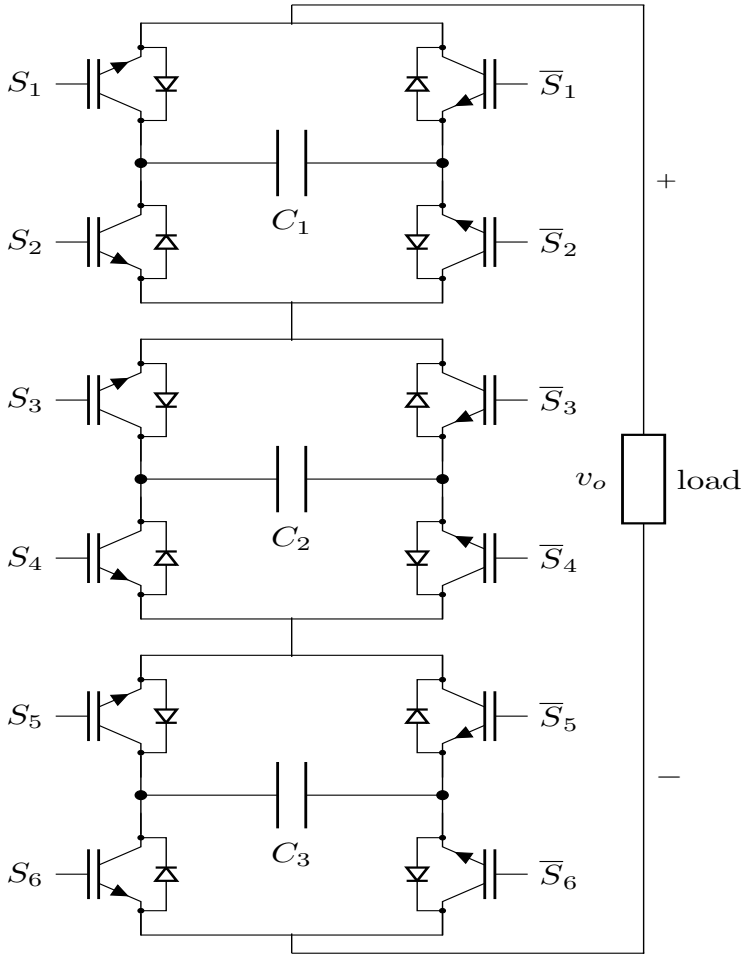


Figure 2.2: Cascaded H-bridge topology consisting of three cells H-bridges.

2.3 Cascaded H-bridges Converter

Figure 2.2 shows the configuration of a 7-level output CHB converter. The converter consists of three H-bridge cells connected in series in order to produce a higher output

voltage. Though the structure makes packing and building such a converter easy, yet this converter requires isolated dc sources, and the capacitor voltages need a special balancing control technique [83–86]. The input dc sources may be equal or may vary according to the application requirements. The CHB is a modular converter, but it needs separate dc supplies that could be provided from a multi-winding phase-shifted transformer, which reduces the power density and increases the system cost. A CHB having N cells can produce 2N+1 output voltage levels including the zero level by utilizing N capacitors and 4N switches.

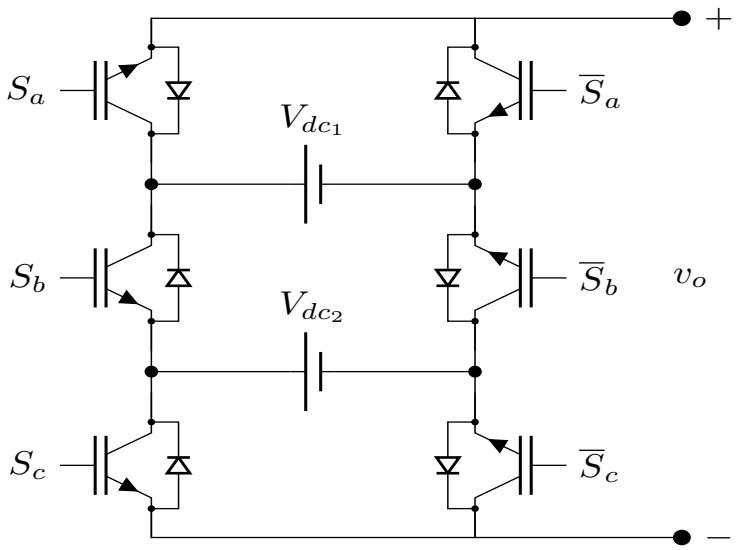


Figure 2.3: Schematic of a 7-Level Packed U-Cell (7L-PUC) converter.

2.4 Packed U-cell Topology

The PUC topology shown in figure 2.3 is considered as a hybrid cascaded H-bridge type of converter. It consist of 6 power switches and two capacitors, resulting in a compact-form MLI structure. One of the capacitors is replaced by a dc source in case of inverter operation mode. The PUC topology introduces a reduction in the number of power switches and the passive elements used in the construction. Table 2.1 shows a comparison between the FCC, CHB and PUC converter topologies in terms of the

number of capacitors and switches for a seven-level output voltage waveform.

Realization of more than five levels in conventional multilevel topologies is a challenging task, due to stability, scalability and modularity limits. However, PUC converter can produce 5- and 7- level output voltages if the second capacitor voltage is controller to half and one-third of the first capacitor dc source, respectively. A higher number of voltage levels implies a small filter size and further reduction in the total harmonic distortion (THD) of the current output in inverter operation mode (or smaller THD of the grid current in rectifier operation mode).

Table 2.1: Comparison table: FCC, CHB and PUC topology devices count for seven levels voltage output.

No. of	FCC	CHB	PUC
Capacitors	6	3	2
Switches	12	12	6

The recently proposed PUC technology brought enormous improvements to MLC technology as compared to the classical MLCs, such as:

- Reduction in the number of passive elements used in the topology.
- Reduction in the number of semiconductor devices, thus reduction in the overall cost.
- Improved AC and DC side power quality without the need for additional bulky harmonic filters.

However, all these benefits brought by the PUC converter are linked to challenges in terms of control complexity; thus PUC has the following disadvantages:

- Bilinear structure, where the control inputs are included in the closed-loop system matrix.

- Control design complexity, where linear and nonlinear control methods cannot be directly applied to the PUC converter.

- Control-associated challenges in terms of modelling and simulations.

Moreover, despite the serious challenges associated with the PUC approach, benefiting from its superior performance and attractive features are worth investing in research work. This will to bring new tools and findings for a better understanding and high performance operation.

2.5 The PUC7 Inverter

A PUC inverter depicted in figure 2.4, has six power switches (S_a, $\overline{S}_a$, S_b, $\overline{S}_b$, S_c, $\overline{S}_c$), one DC source, and one auxiliary capacitor, with their voltages denoted as V_{dc} and v_c, respectively. Switches are controlled as complementary pairs with their switching states defined as,

$$s_k = \begin{cases} 1 & \text{if } S_k \text{ is closed } (\overline{S}_k \text{ is open}) \\ 0 & \text{if } S_k \text{ is open } (\overline{S}_k \text{ is closed}) \end{cases}$$

where $k \in \{a, b, c\}$.

The PUC single-phase inverter is connected to the utility grid through a line filter with inductance value designated as L_g, and its parasitic resistance as r_g. The inverter's control objective is to inject to the grid, at a controlled power factor, a sinusoidal current i_g, which follows a current reference i_g^*. This can be accomplished by designing a controller, which selects the proper switching states for the converter so current is injected to the grid at minimum THD, while keeping the capacitor voltage close to its reference value v_c^*.

The far right column of Table 2.2 refers to the charging state of the capacitor with

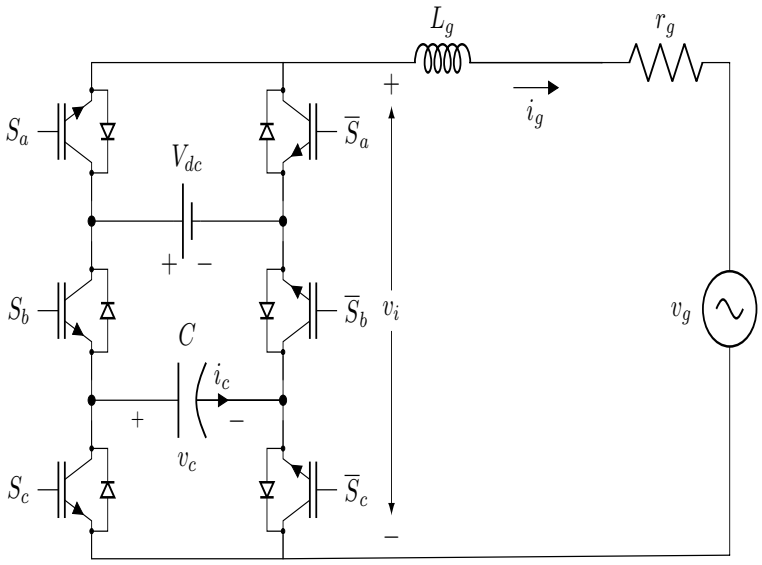


Figure 2.4: Grid-connected PUC7 inverter.

respect to the grid current direction and the applied switching state. The symbols used are (↑: charging), (↓: discharging), and (⌣: no change). The pair of switching functions (s_1, s_2) are defined as

$$\begin{aligned} s_1 &= s_a - s_b \\ s_2 &= s_b - s_c \end{aligned} \tag{2.1}$$

Using Table 2.2 and (2.1), the inverter output voltage can be written as,

$$v_i = s_1 V_{dc} + s_2 v_c \tag{2.2}$$

The capacitor dynamics is expressed as,

$$i_c = C\frac{dv_c}{dt} = -s_2 i_g, \tag{2.3}$$

Table 2.2: PUC7 Switching States And Terminal Voltages

l	s_1	s_2	s_a	s_b	s_c	v_i	$v_i\Big\vert_{v_c=E}^{V_{dc}=3E}$	$i_g>0$	$i_g<0$
1	+1	0	1	0	0	V_{dc}	$3E$	$\backsim$	$\backsim$
2	+1	−1	1	0	1	$V_{dc}-v_c$	$2E$	$\uparrow$	$\downarrow$
3	0	+1	1	1	0	v_c	E	$\downarrow$	$\uparrow$
4	0	0	1	1	1	0	0	$\backsim$	$\backsim$
	0	0	0	0	0	0	0	$\backsim$	$\backsim$
5	0	−1	0	0	1	$-v_c$	$-E$	$\uparrow$	$\downarrow$
6	−1	1	0	1	0	$-V_{dc}+v_c$	$-2E$	$\downarrow$	$\uparrow$
7	−1	0	0	1	1	$-V_{dc}$	$-3E$	$\backsim$	$\backsim$

while the grid model and the current dynamics can be written as

$$\frac{di_g}{dt} = -\frac{r_g}{L_g} i_g + \frac{1}{L_g}\left(v_i - v_g\right). \tag{2.4}$$

One can define the grid current error as $x_1 = i_g - i_g^*$, where i_g^* represents the grid current reference signal. Similarly, the capacitor voltage error may be defined as $x_2 = v_c - v_c^*$, where $v_c^* = E$ is a constant DC voltage reference for the capacitor. In this seven-level PUC inverter, the DC reference voltage (E) is taken to be one-third of the DC supply voltage $V_{dc} = 3E$, in order to produce 7-level inverter output voltage. From the above equations the current error derivative can be written as

$$\begin{aligned} \dot{x}_1 &= \frac{di_g}{dt} - \frac{di_g^*}{dt} \\ &= \frac{1}{L_g}\left\{ s_1 V_{dc} + s_2 v_c - \left(v_g + r_g i_g + L_g \frac{di_g^*}{dt} \right) \right\} \end{aligned} \tag{2.5}$$

Using $i_g = x_1 + i_g^*$, and $v_c = x_2 + v_c^*$, one can obtain,

$$\dot{x}_1 = \frac{1}{L_g}\left\{ s_1 V_{dc} + s_2\left(x_2 + v_c^*\right) - r_g x_1 - v_i^* \right\} \tag{2.6}$$

One can define the reference voltage of the grid inverter output v_i^* as,

$$v_i^* = v_g + r_g i_g^* + L_g \frac{di_g^*}{dt} \tag{2.7}$$

Similarly, after substituting the expression of $i_g = x_1 + i_g^*$ in (2.3), the capacitor voltage error may be written as,

$$\dot{x}_2 = -\frac{1}{C} s_2 \left(x_1 + i_g^* \right) \tag{2.8}$$

In the next Chapter, derivation of the inverter control law is mathematically developed and thoroughly discussed.

Chapter 3

LYAPUNOV-BASED MODEL PREDICTIVE CONTROL OF A PUC7 GRID-CONNECTED MULTILEVEL INVERTER

3.1 Introduction

In this chapter a model-based predictive control method with a cost function derived intuitively from Lyapunov's control theory is presented. Furthermore, the selection process of cost function gains is omitted in the proposed method. Thus the proposed cost function eliminates the need for optimization and tuning of the weighting factors associated with the states error. Due to the usage of a Lyapunov-based cost function, stability of the controlled system is guaranteed. A robustness study is presented, simulations and experimental results show the effectiveness of the proposed control scheme, which achieves a fast dynamic response, robust performance, and low-THD grid current.

3.2 Lyapunov-Based Controller Design

3.2.1 Theory Overview

Mathematical model of the PUC grid connected inverter is given in Section 2.5. Lyapunov direct method of stability is a tool to study the stability of the controlled system by examining the variation of an "energy-like" scalar function, called Lyapunov function $V(\mathbf{x})$. This method has shown its effectiveness in the applications

of power electronics, where disturbances and robustness are the main keys to ensure power quality to the controlled system [87]. The Lyapunov function can be defined in terms of system state errors, represented by the vector $\mathbf{x}$. Assume that the equilibrium of controlled system is at the origin $\mathbf{x} = \mathbf{0}$. When the energy function becomes zero, the system is settled at the equilibrium point, and if the energy function is rapidly increasing, then the system is unstable, and is asymptotically stable if energy is decreasing. The stability of a system is guaranteed if the following conditions hold [88]:

1) $V(\mathbf{x})$ is positive definite.

2) $\dot{V}(\mathbf{x})$ is negative definite.

3) $V(\mathbf{x})$ goes to ∞ as $\|\mathbf{x}\| \to \infty$.

Geometrically, condition 1) implies that the Lyapunov function is a bowl-like function upward, with minimum at the equilibrium point. Condition 2) implies that the rate of energy change will drive the state towards the equilibrium point. The last condition assures that error state is located on a closed contour around the equilibrium point.

3.2.2 Error Function Evaluation

The design goal is to simultaneously control the injected grid current as well as the capacitor voltage. In order to achieve this goal, a Lyapunov function in terms of system's errors is suggested as the following,

$$V(\mathbf{x}) = \frac{1}{2}\alpha_1 x_1^2 + \frac{1}{2}\alpha_2 x_2^2 \tag{3.1}$$

where α_1 and α_2 are real positive numbers, which must be properly selected. It is clear that the above function is positive definite. Lyapunov control theory states that, stability of the controlled system presented by (2.3) and (2.4) is guaranteed if we insure

that for all values of **x**,

$$\dot{V}(\mathbf{x}) < 0 \tag{3.2}$$

Derivative of (3.1) with respect to time yields,

$$\dot{V}(\mathbf{x}) = \alpha_1 x_1 \dot{x}_1 + \alpha_2 x_2 \dot{x}_2. \tag{3.3}$$

Using equations (2.6) and (2.8) in (3.3) one can get,

$$\begin{aligned} \dot{V}(\mathbf{x}) = \frac{1}{L_g} s_2 x_1 x_2 \left(\alpha_1 - \frac{L_g}{C} \alpha_2 \right) - \frac{\alpha_2}{C} x_2 s_2 i_g^* \\ + \frac{\alpha_1}{L_g} x_1 \left(s_1 V_{dc} + s_2 v_c^* - r_g x_1 - v_i^* \right). \end{aligned} \tag{3.4}$$

In order to eliminate the $x_1 x_2$-term in (3.4), gains are chosen to satisfy $\alpha_1 = \frac{L_g}{C} \alpha_2$. Accordingly, (3.4) reduces to,

$$\dot{V}(\mathbf{x}) = \frac{\alpha_1}{L_g} \{ x_1 \left(s_1 V_{dc} + s_2 v_c^* - r_g x_1 - v_i^* \right) - x_2 s_2 i_g^* \}. \tag{3.5}$$

Equation (3.5) is used to select the control switches pair (s_1, s_2) such that the derivative of the cost function is generally negative.

3.3 Lyapunov-Based MPC Design

In this section, a model-based predictive controller is derived in discrete-time, based on the derivative of the Lyapunov function in (3.5). Note that (3.5) gives the Lyapunov function derivative in continuous time, with piece-wise constant switching function pair (s_1, s_2). Therefore, in order to derive the switching functions that will be applied in the interval $(kT_s, (k+1)T_s)$, such that the derivative is negative at the end of this interval, prediction of the derivative at $(k+1)T_s$ is required. A Phase-Locked-Loop (PLL) is used to track and extract grid voltage information. Then a grid current reference signal is created with an appropriate phase shift with respect

to the grid voltage. Usually, a high level controller generates the grid current reference, given the active and reactive powers to be injected into the grid. Moreover, system states (v_c, i_g) and grid voltage v_g are all measured at instant (k). Next, prediction of the states at $(k+1)$ is made, and the state errors at time instant $(k+1)$ are calculated. The switching pair is chosen to minimize the derivative of the Lyapunov function given in (3.5). In the following sections, these calculations are described in detail.

3.3.1 System States Prediction

Using the first order forward Euler approximation, capacitor voltage and grid current in (2.3) and (2.4) are written in discrete form as follows,

$$\begin{aligned} v_c(k+1) &= v_c(k) - \frac{T_s}{C} i_g(k) s_2(k) \\ i_g(k+1) &= \lambda i_g(k) + \frac{T_s}{L_g}\Big(v_i(k) - v_g(k)\Big), \end{aligned} \tag{3.6}$$

where $\lambda = (1 - r_g T_s / L_g)$. Equation (3.6) is used to predict the states at $(k+1)$ using variable values at time (k). In addition, one needs to extrapolate the reference current value at $(k+1)$. The first order linear interpolation by means of averaging the previous values is used, as follows,

$$\begin{aligned} v_g(k+1) &= \frac{3}{2} v_g(k) - \frac{1}{2} v_g(k-1) \\ i_g^*(k+1) &= \frac{3}{2} i_g^*(k) - \frac{1}{2} i_g^*(k-1). \end{aligned} \tag{3.7}$$

Furthermore the inverter reference voltage at $(k+1)$ is predicted as,

$$v_i^*(k+1) = v_g(k+1) + r_g i_g^*(k+1) + \frac{L_g}{T_s}\{i_g^*(k+1) - i_g^*(k)\}. \tag{3.8}$$

Making use of (3.6) and the definition of the errors, the grid current error at the time

instant$(k+1)$ is given by

$$\begin{aligned} x_1(k+1) &= i_g(k+1) - i_g^*(k+1) \\ &= \frac{T_s}{L_g}\left(\frac{L_g}{T_s}\lambda x_1(k) + s_1(k)V_{dc} + s_2(k)\left[x_2(k) + v_c^*\right]\right) \\ &+ Q(k), \end{aligned} \tag{3.9}$$

The term $Q(k)$ is independent from the states and the control input, and given as

$$Q(k) = \lambda i_g^*(k) - \frac{T_s}{L_g} v_g(k) - i_g^*(k+1). \tag{3.10}$$

Similarly, the capacitor voltage error at $(k+1)$ can be found as

$$\begin{aligned} x_2(k+1) &= v_c(k+1) - v_c^* \\ &= x_2(k) - \frac{T_s}{C} x_1(k) s_2(k) - \frac{T_s}{C} i_g^*(k) s_2(k). \end{aligned} \tag{3.11}$$

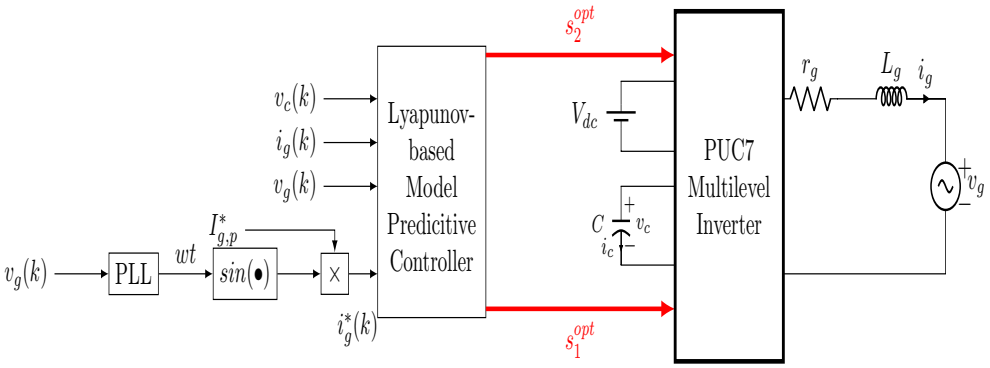


Figure 3.1: Block diagram of the proposed Lyapunov-based MPC controller.

3.3.2 Lyapunov Cost Function and The Control Algorithm

From now on, the derivative of Lyapunov function will be referred to as the cost function. The cost function used in this algorithm is evaluated for the next sampling instant (k+1) based on (3.5). The predicted variables from (3.7) - (3.11) are used to determine the errors of the state variables at (k+1). The control block diagram is shown in figure 3.1. After measuring the states of the controlled system, and

Algorithm 1 Lyapunov-based MPC algorithm for PUC7 grid-connected inverter

1: Measure $v_g(k), i_g(k), v_c(k)$
2: Calculate (3.7) and (3.8). ▷ prediction of v_g, i_g and v_i^*
3: **for** $l = 1 \ldots 7$ **do**
4: Calculate (3.9) and (3.11). ▷ calculating the errors at $(k+1)$ time instant.
5: Evaluate (3.12). ▷ evaluating the cost function.
6: **return** minimum $\dot{V}_{\mathbf{x}}(k+1)$
7: Choose the switching pair for which $\dot{V}_x(k+1)$ is minimum

predicting the state values at instance $((k+1)$, errors at time instant $(k+1)$ are determined. Evaluating equation (3.5) at the time instant (k+1) yields,

$$\begin{aligned}\dot{V}_{\mathbf{x}}^{(l)}(k+1)=\frac{\alpha_1}{L_g}\Big\{x_1(k+1)\{s_1^{(l)}(k)V_{dc}+s_2^{(l)}(k)v_c^*-r_g x_1(k+1)\\ -v_i^*(k+1)\}-x_2(k+1)s_2^{(l)}(k)i_g^*(k+1)\Big\}.\end{aligned} \tag{3.12}$$

where l refers to the level index in Table 2.2 in Section 2.5. At time step (k) the control algorithm works as shown in Algorithm 1. It is worth mentioning that the controller targets the minimum of the Lyapunov function $V(\mathbf{x})$. Further detailed discussion is entailed in Section 3.3.3. The main advantage of the proposed controller is that there are no gains to be tuned for optimizing the performance. Therefore, a unique performance is expected from this controller. Another main feature is its good robustness against parameter variations, as will be shown in the following sections.

3.3.3 Stability Analysis

Although predictive control offers superior performance as compared to classical control methods for many power electronics control problems, it still lacks studies on stability and robustness analysis [52, 53]. In this work, the choice of a control strategy based on Lyapunov theory helps to study the stability of the controlled system. In standard Lyapunov theory the stability analysis is done by first finding a positive definite Lyapunov function; then the derivative of this function is proved to be negative definite [88]. This guarantees that the system trajectory is such that the

Lyapunov function decreases, which becomes zero at the equilibrium point. However, the classical approach in Lyapunov stability analysis can't be applied to the problem here because of the followings: 1) the control variables are switching signals, 2) the set of discrete control variables involves a large number of elements (seven elements). Therefore, the analysis approach we adopted is less rigorous than the common Lyapunov practice. At this step, assume $r_g = 0$ and substitute (3.9) and (3.11) in (3.12) then one obtains

$$\begin{aligned}
&\dot{V}_{\mathbf{x}}(k+1) \\
&= \frac{\alpha_1}{L_g}\left\{\frac{T_s}{L_g}\left(\frac{L_g}{T_s}\lambda x_1(k) + s_1(k)V_{dc} + s_2(k)\left(x_2(k) + v_c^*\right)\right)\right. \\
&\left. + Q(k)\right\}\left(s_1(k)V_{dc} + s_2(k)v_c^* - v_i^*(k+1)\right) - \frac{\alpha_1}{L_g}\left\{x_2(k)\right. \\
&\left. - \frac{T_s}{C}x_1(k)s_2(k) - \frac{T_s}{C}i_g^*(k)s_2(k)\right\}i_g^*(k+1)s_2(k)
\end{aligned} \tag{3.13}$$

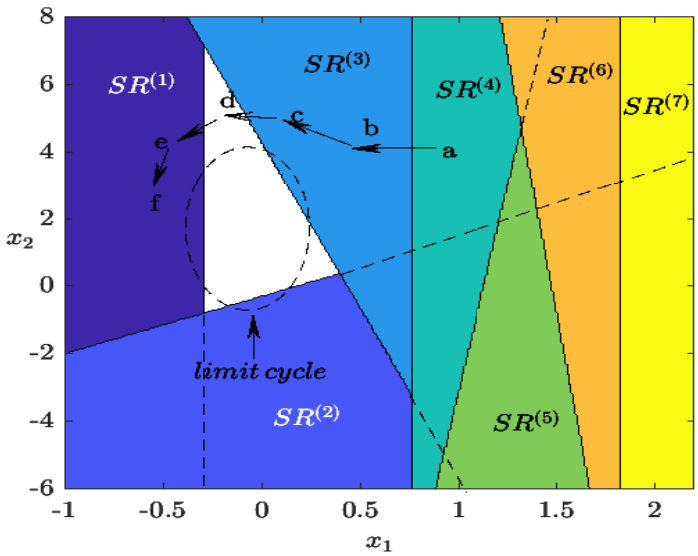


Figure 3.2: Stability region comprised of half-planes corresponding to all switching inputs.

The term α_1/L_g multiplies both terms in (3.13), so it can be eliminated from the equation because it has no influence on the decision of stability. After eliminating that

term, (3.13) can be written in the following form

$$\dot{V}_{\mathbf{x}}(k+1) = a(k)x_1(k) + b(k)x_2(k) + c(k) \tag{3.14}$$

where

$$\begin{aligned}
a(k) &= \lambda V_{bias} + \frac{T_s}{C} s_2^2(k) i_g^*(k+1) \\
b(k) &= \frac{T_s}{L_g} s_2(k) V_{bias} - s_2(k) i_g^*(k+1) \\
c(k) &= \Big(Q(k) + \frac{T_s}{L_g} \{ s_1(k) V_{dc} + s_2(k) v_c^* \} \Big) V_{bias} \\
&\quad + \frac{T_s}{C} s_2^2(k) i_g^*(k) i_g^*(k+1) \\
V_{bias} &= s_1(k) V_{dc} + s_2(k) v_c^* - v_i^*(k+1)
\end{aligned} \tag{3.15}$$

It is clear from (3.14) that the derivative of the Lyapunov function is a time-varying function. In this control problem we have only seven control inputs, each corresponding to an inverter output voltage. The output levels are indicated by the index $l = 1 \ldots 7$ as given in Table 2.2. Corresponding to the control inputs, stability regions on the x_1x_2-plane are defined as

$$SR^{(l)}(k+1) = \{(x_1, x_2) \mid \dot{V}_{\mathbf{x}}^{(l)}(k+1) < 0\}. \tag{3.16}$$

Note that each of the stability regions is a half-plane on the x_1x_2-plane. For instance, $SR^{(1)}(k+1)$ refers to the stability region on the x_1x_2-plane when the control pair $(+1, 0)$ is applied. The inverter output voltage for this case is $v_i = 3E$ in the steady state. By examining equations (3.8)-(3.11), it is obvious that these functions are time varying functions and they are all involved in calculating (3.12), which is again time varying function. [1]

[1] Please refer to the animation files provided with this thesis, which shows the stability regions for one complete cycle.

Refer to figure 3.2, the regions $SR^{(l)}(k+1)$, $l = 1 \ldots 7$ are shown as the colored half-planes, where the white region does not belong to any of these regions, hence $\dot{V}_{\mathbf{x}}(k+1)$ is positive herein. Given a point $'a'$ on the state plane outside the white region, it can be seen that this point belongs to at least one of the stability regions. In this case the controller chooses the control pair for which $\dot{V}_{\mathbf{x}}(k+1)$ is minimum (most negative). After control input application the state will be driven in such a direction that the Lyapunov function decreases. This corresponds to the trajectory being directed toward the origin shown as the sequence of points $'a', \ldots, 'f'$. Eventually, the trajectory will enter a limit cycle . At this stage, it is important to note that the state errors are in general periodic functions of time (in the steady state). This can be understood by examining equations (3.9) and (3.11). The implication is that the equilibrium of the system is not a single point but a limit cycle.

In case the state enters the white region where $\dot{V}_{\mathbf{x}}(k+1)$ is positive, the trajectory will be forced to leave this region and enter the limit cycle. It should be noted that in the steady state the average of $\dot{V}_{\mathbf{x}}(k)$ over one period is zero. A nonzero average value would imply an increasing or decreasing Lyapunov function which is impossible if the system is stable. To maintain zero average for $\dot{V}_{\mathbf{x}}(k)$ in the steady state, part of the system trajectory should be within the colored regions and the rest in the white region as shown in figure 3.2. Notice that the trajectory will not circle a static region, as shown in the figure, but instead a time-varying region (as shown in the gifs provided with the thesis). An important point to mention here, is that the stability discussions above are valid for any set of system parameters. Using different parameters will only change the regions to a certain degree but the concepts discussed will remain the same.

In order to show the system's stability, it is required to show that the unstable region is

encompassed by many stable regions under all conditions. By doing so, we will ensure that if the state is in the stability region/s the trajectory will be in such a direction as to decrease $\dot{V}_{\mathbf{x}}(k)$, and if the state is in the unstable region the state will be directed to the stable region. This is the case even though the stability region is time varying. In conclusion, the system is only stable in the sense of Lyapunov if the unstable region is always closed by different stable regions. The presented analysis, simulation and experimental results show that the stability is verified. Yet, the authors believe that a full mathematical demonstration is still an open topic in a new research work.

3.4 Robustness Analysis

In order to prove robustness of the proposed controller, the system's response has been studied under the effect of capacitor mismatch, as shown in figure 3.3. Simulations are performed for system parameters given in Table 3.1, with the exception that sampling time is chosen as $T_s = 25\,\mu s$ at 10A peak reference grid current. The controller employs an estimated value of the capacitance, denoted as C_{est}, which is different from actual capacitor value, denoted as C_{act}, where $\Delta C_2(\%) = \frac{C_{act} - C_{est}}{C_{act}} \times 100$. As shown in figure 3.3, grid current THD is almost invariant under capacitance mismatch, while capacitor voltage RMS error is slowly increasing as estimated capacitance value increases. The average switching frequency, however, increases up to 17.2 kHz when capacitance mismatch reaches -50%.

Similarly, when a mismatch is applied to the filter inductance value L_g, the THD of grid current is observed to increase as L_{est} becomes greater than L_{act}, as shown in figure 3.4, where $\Delta L_g(\%) = \frac{L_{act} - L_{est}}{L_{act}} \times 100$. Also, a similar behavior is noticed for average switching frequency which increases up to 17 kHz for -50% mismatch in L_g.

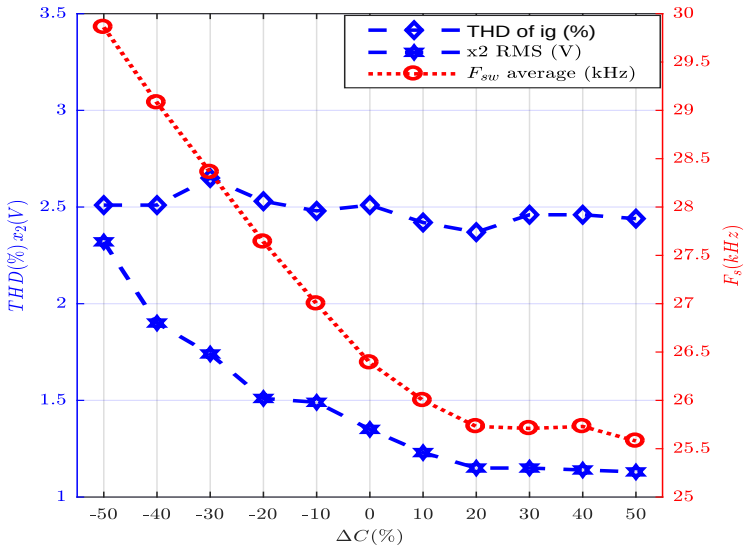


Figure 3.3: Capacitance value mismatch versus average switching frequency, grid current total harmonic distortion and capacitor voltage RMS error. (T_s=25μs).

From figure 3.4, it can be shown that the distortion of grid current is linked to the mismatch in grid inductance value. On the other hand, a mismatch in the inductance value shows a negligible influence on the capacitor voltage RMS error.

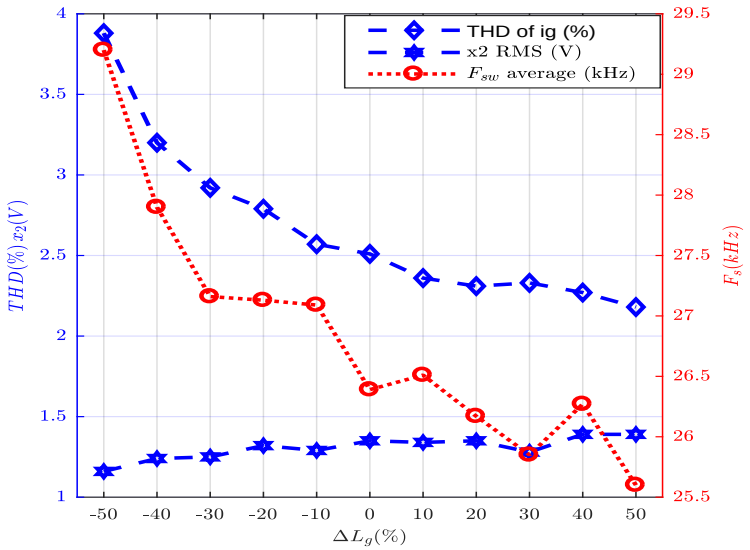


Figure 3.4: Inductance value mismatch versus average switching frequency, grid current total harmonic distortion and capacitor voltage RMS error. (T_s=25μs).

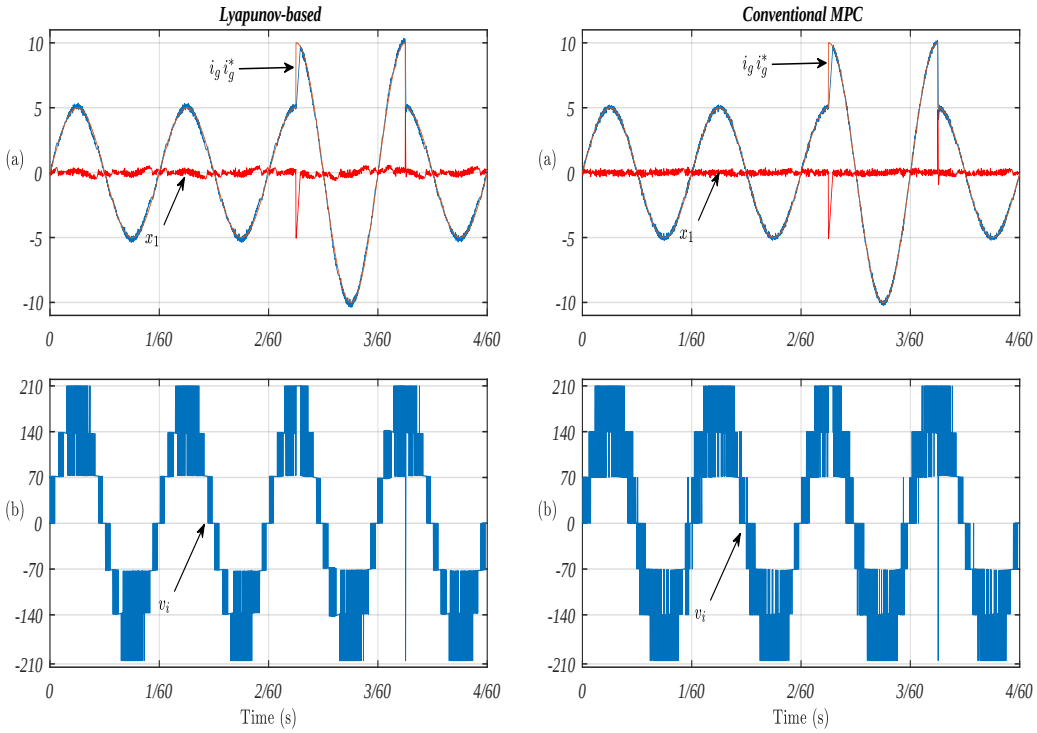


Figure 3.5: Steady state and dynamic response comparison of conventional MPC in [1] and proposed MPC. (top): grid current, grid current reference and the error x_1 (A), (bottom): 7-level inverter output voltage v_i (V).

3.5 Comparison with classical MPC

The proposed controller is compared with another MPC-based method. The authors in [1] have suggested a model based predictive controller with the following normalized cost function,

$$g = \lambda \frac{x_2}{\Delta v_{c,\max}} + \frac{x_1}{\Delta i_{g,\max}} \tag{3.17}$$

where $\Delta v_{c,\max} = 2 i_g T_s / C$ and $\Delta i_{g,\max} = 2 V_{dc} T_s / L_g$. The parameter λ is a positive gain associated with the capacitor error, and it should be chosen properly in order to maintain both, low capacitor voltage error and low THD of grid current. The THD of the grid current is defined as

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \ldots}}{I_1^2} \tag{3.18}$$

where I_n is the RMS value of the nth harmonic current, and n=1 is the fundamental component. The RMS value of the capacitor voltage error is defined as

$$x_2\,(\text{RMS}) = \sqrt{\frac{1}{T}\int_0^T x_2^2 dt} \tag{3.19}$$

Where T is the fundamental period of the grid voltage. Authors in [1] suggest a method to properly choose the gain. The same method is used in this work to obtain the optimal λ value suitable for system used in the experimental setup. Applying method used in [1] yields $\lambda = 0.149$, which is used in this comparison test. Figure 3.5 shows steady state and dynamic performance comparison between conventional MPC and the proposed MPC. The steady state performance is shown in the first two cycles and the dynamic performance is shown in the last two cycles due to a step change in current reference.

Table 3.1: Simulation and Experimental Parameters

Parameters	Symbol	Value
Dc voltage source	V_{dc}	210V
Inverter capacitance	C	1.5mF
Grid voltage (RMS) and frequency	V_g,f_g	120V, 60Hz
Grid inductance and resistance	L_g,r_g	5mH, 0.7Ω
Sampling time	T_s	25μs

The grid current THD and the average switching frequency ($F_{s,\text{av}}$) are compared, whereas the capacitor voltage error is kept equal for both methods. The comparison is performed for 10A peak reference current with the system parameter listed in Table 3.1. A summary of the comparative test is listed in Table 3.2.

Although the proposed method has slightly higher THD, as compared to the control

Table 3.2: Comparison table: Classical MPC vs Proposed Method

Parameters	Classical MPC [1]	Lyapunov-based MPC
THD of i_g(%)	2.10	2.51
$F_{s,av}$ (kHz)	33.24	26.39
x_2 RMS (V)	1.35	1.36
Gain tuning	gain is involved (tuning is required)	no gain involved (simple)

method in [1], it has two fundamental advantages, which includes lower switching frequency and ease of implementation. Moreover, in the proposed method, there is no need to tune any gains like λ. In the method proposed in [1], λ needs to be tuned for different grid current references, different sampling time, or new system parameters. On the other hand, in this proposed control method, the derivative function in (3.5) does not involve any tunable parameters.

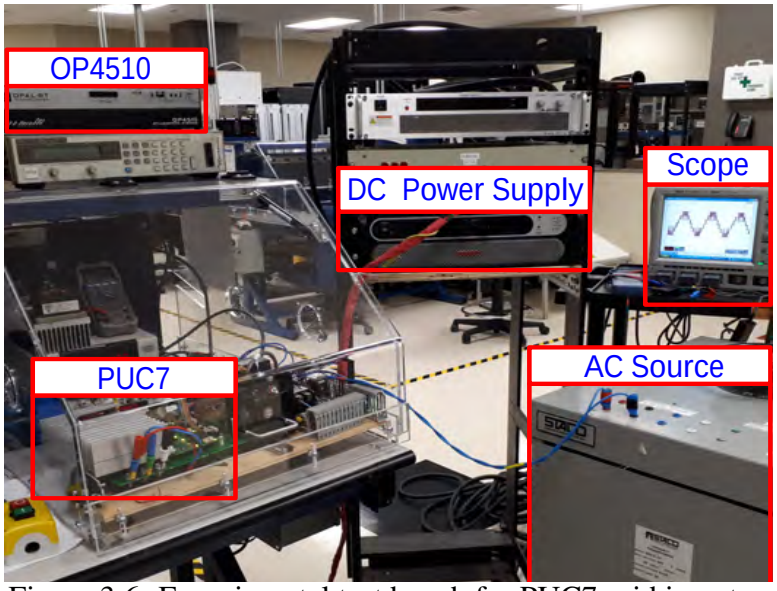


Figure 3.6: Experimental test bench for PUC7 grid inverter.

3.6 Simulation and Experimental Results

In order to verify the behavior of the proposed scheme, various simulation scenarios of the 1.5 kVA single-phase grid-connected PUC7 system using SimPowerSystem library from Simulink/MATLAB along with experimental tests have been carried out.

Figure 3.6 shows the test-bench of the experimental setup. The proposed control algorithm is running on the OP4510 real-time controller from OPAL-RT. Specifications and parameters of the controlled system are listed in Table 3.1 for both simulation and experimental tests.

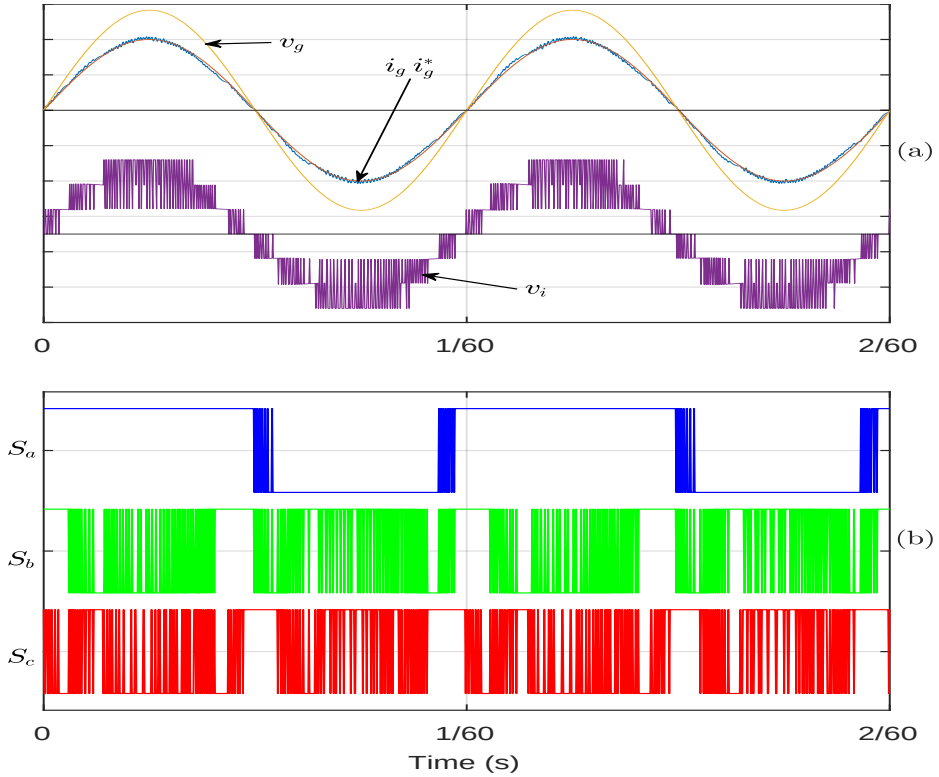


Figure 3.7: Simulation results during a steady state injection of active power into the grid. (a) Grid voltage (60V/div), grid current and its reference (5A/div), and inverter output voltage (100V/div). (b) Switching control signals of the three pairs of switches.

3.6.1 Steady State Test

Depicted in figure 3.7 are simulation results showing the low THD of grid current achieved by the proposed control method. Grid current THD is calculated as 2.51% for 10A peak of reference grid current. The capacitor voltage output wave-forms for simulation and experimental tests are given in figure 3.8. The RMS error of the capacitor voltage is 1.36V in the simulation results. Average switching frequency was

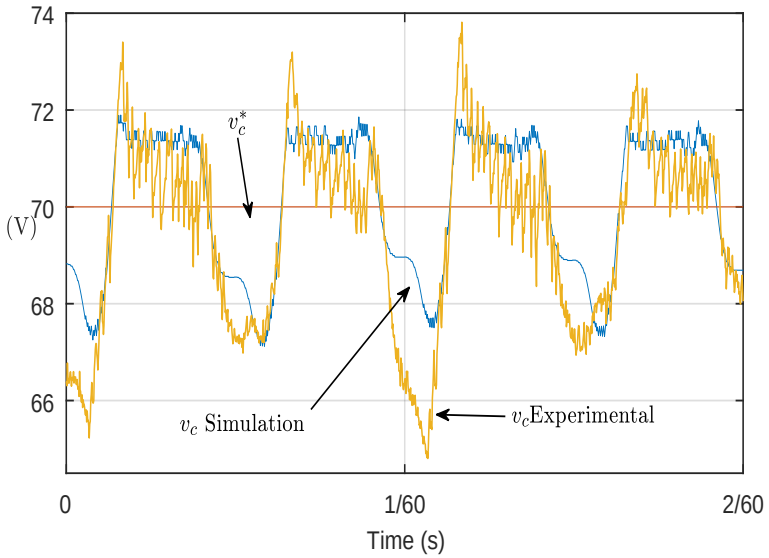


Figure 3.8: Simulation and experimental results (corresponds to figure 3.7) of capacitor voltage during a steady state injection of active power into the grid (10A peak current reference).

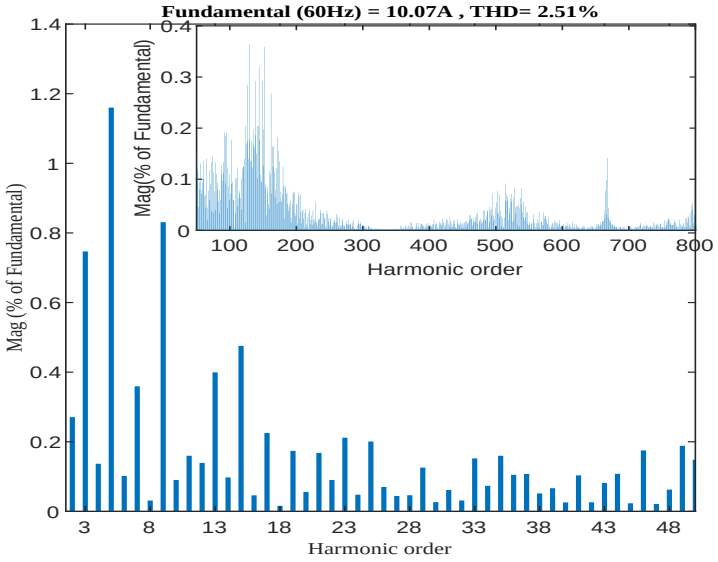


Figure 3.9: Harmonic spectrum of grid current with respect to the fundamental component.

found to be 26.39 kHz. The average switching frequency is calculated as,

$$F_{s,\text{av}} = \frac{N_{S_a} + N_{S_b} + N_{S_c}}{T_{\text{total}}} \tag{3.20}$$

where N_{S_a}, N_{S_b} , and N_{S_c} represent the total number of times the devices switch in a time interval of T_{total}, counting turn ON and turn OFF as two separate switching events. For example, when the simulation is run for 10 fundamental periods ($T_{\text{total}} = 10/60$),

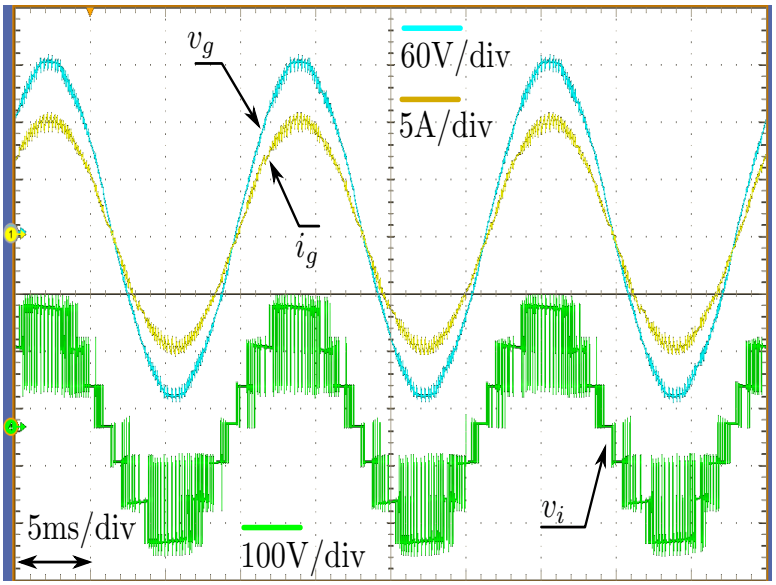


Figure 3.10: Experimental results during a steady state injection of active power into the grid.

the devices switch ON and OFF 262, 2104 and 2033 times, respectively.

Figure 3.9 shows the calculated harmonic spectrum of the grid current from simulation results of figure 3.7. Moreover, figure 3.10 shows the experimentally measured voltage and current waveforms of the inverter-grid system at steady-state, with grid current THD measured as 3.57%.

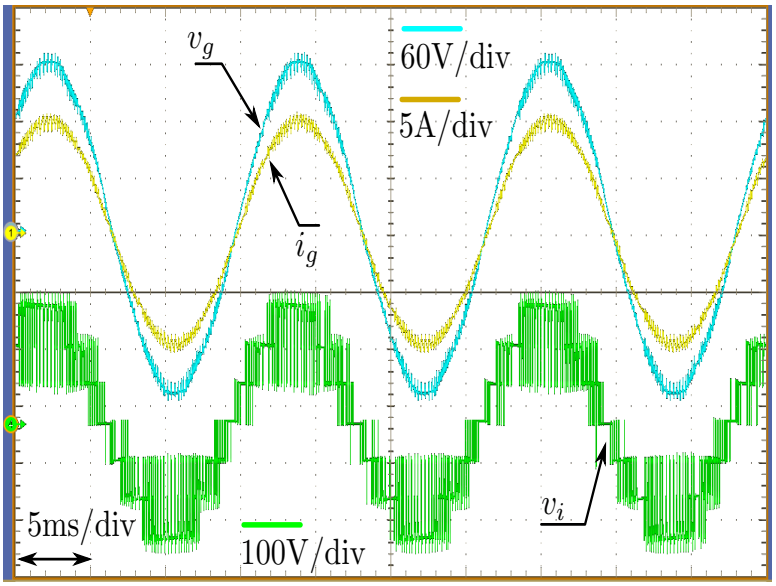


Figure 3.11: Experimental results during a steady state injection of active power into the grid, with $+30\%$ mismatch in L_g.

3.6.2 Parameter Mismatch Test

The robustness of the controller is also tested in the experimental system against parameter mismatches. Figure 3.11 shows the measured system waveforms, with a grid current THD measured as low as 3.81%. Similarly, figure 3.12 shows the output waveforms when there is a mismatch in the capacitance value. The output grid current THD is measured as 3.37%. In all the experimental results, it is clear that all 7-Levels of inverter output voltage are well maintained.

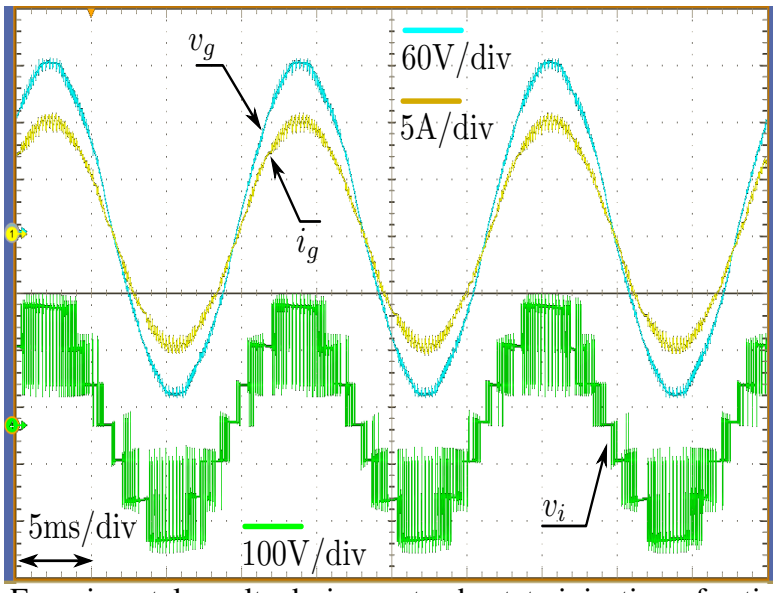


Figure 3.12: Experimental results during a steady state injection of active power into the grid, with +30% mismatch in C.

3.6.3 Dynamic Response Test

Dynamic response of the controller is measured by applying a step change in the grid current reference amplitude. As can be seen in figure 3.13, the grid current reference amplitude was increased from 5A to 10A peak, corresponding to 100% increase in grid current amplitude, then after 2 fundamental cycles the grid current reference amplitude was reduced back from 10A to 5A. The controller exhibits a fast response

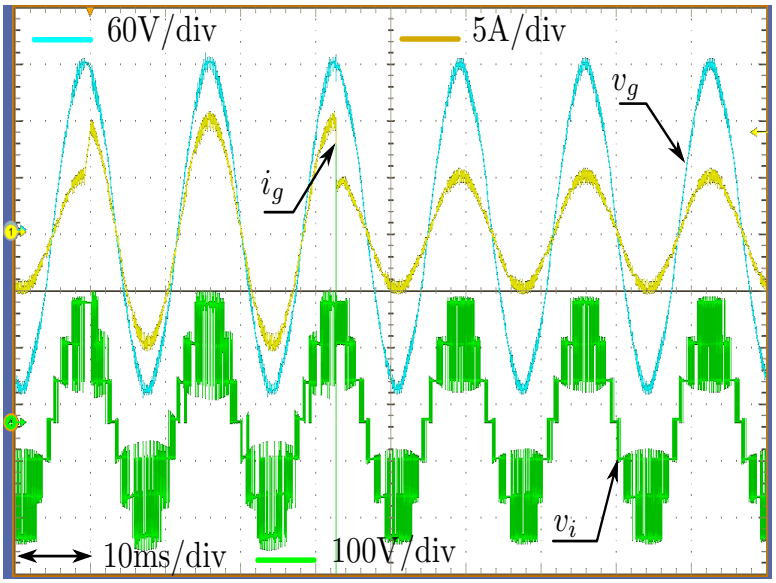


Figure 3.13: Experimental results during a 100% step change in current reference within 2 fundamental cycles.

to the step change in grid current reference, while maintaining a unity power factor power injection to the grid.

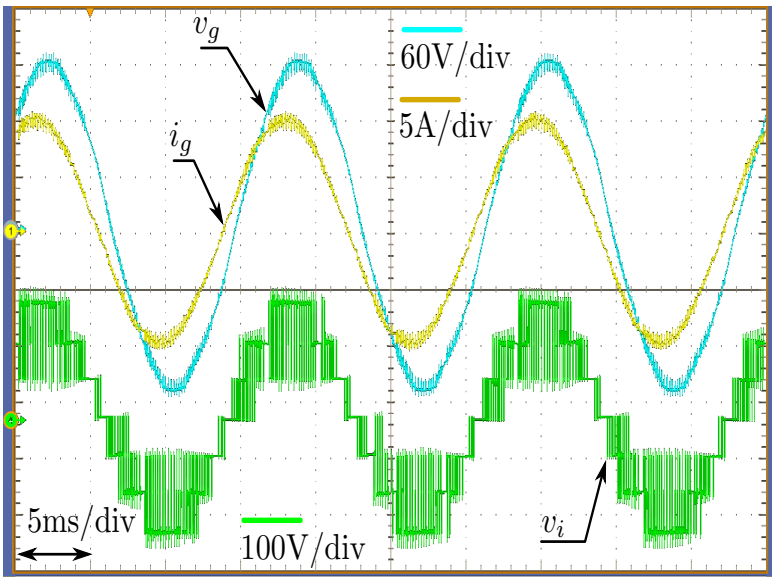


Figure 3.14: Experimental results showing inverter and grid voltages, with grid current leading by 20°.

3.6.4 Active and Reactive Power Flow Tests

After the grid voltage is phase locked, a current reference is calculated with a desired amplitude and phase shift, to resemble the desired active and reactive power injected

into the grid. Figure 3.14 shows experimental results corresponding to a leading power factor. The grid current reference is 20° leading the grid voltage. The grid current total harmonic distortion was measured as 3.88%. Figure 3.15 shows experimental results for the lagging power factor case, where the current reference lags the grid voltage by 20°, with grid current THD measured as 3.04%.

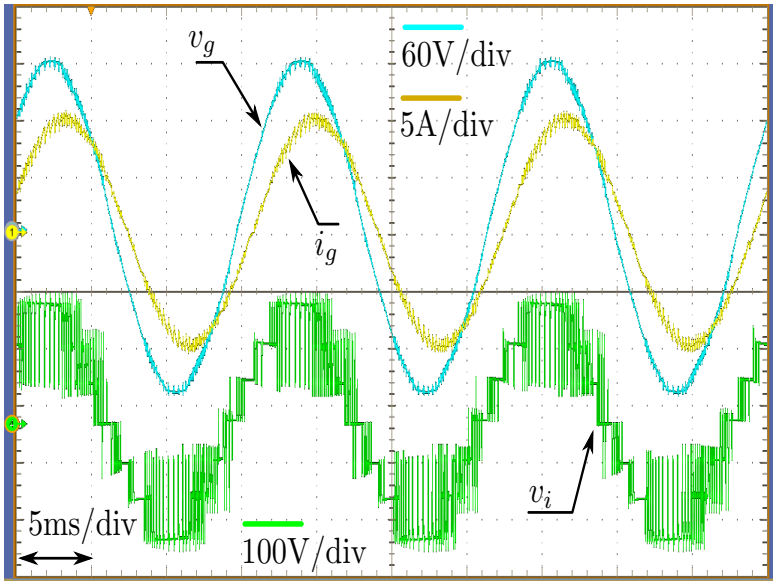


Figure 3.15: Experimental results showing inverter and grid voltages, with grid current lagging by 20°.

3.7 Conclusions

In this chapter, a new model-based predictive controller is presented. The proposed control scheme uses a cost function derived from Lyapunov control theory, which is applied to a multi-level PUC grid connected inverter. The proposed cost function is compared to a weight-structured cost function, and it has the following advantages: 1) lower average switching frequency, 2) parameter tuning not required, and 3) ease of implementation. Results from both simulation and experimental tests, using the proposed controller, demonstrate the excellent performance in terms of harmonic distortion, immunity to parameter mismatch, and robustness against disturbances.

Chapter 4

AN EFFECTIVE SLIDING MODE CONTROL DESIGN FOR A GRID-CONNECTED PUC7 MULTILEVEL INVERTER

4.1 Introduction

In this chapter, an effective and robust finite-control-set sliding mode controller is introduced. In alignment with the dual control objective of the capacitor voltage and the grid current, two separate sliding functions are designed (one sliding function for each state error). The control is established by choosing the control input in order to satisfy the reaching conditions of both sliding functions. This is achieved by checking all possible control pairs for the two cost functions derived to ensure the stability of the reaching mode. Compared to the existing control methods, the proposed control method has the following advantages: 1) simple in design and implementation; 2) No parameter tuning is required; 3) Low computational complexity; 4) Introduction of a hysteresis bandwidth (h) for the capacitor voltage, which permits further reduction of the average switching frequency. The hysteresis bandwidth directly links the error in the capacitor voltage to the parameter value h. The remaining part of this chapter is organized as follows: the mathematical modeling of the PUC7 inverter topology is presented in Section 2.5. In Section 4.2, the sliding mode controller is discussed including an assessment of its stability. In Section 4.3, experimental results are presented and analyzed to conclude about the performance of the proposed technique.

A comprehensive comparison with the MPC method is given in Section 4.4. Finally, Section 4.5 concludes the chapter.

4.2 SMC Design

4.2.1 SMC Design Challenge

In this section, the sliding mode based controller design is presented. The design of the SMC involves:

a. Designing a proper switching (sliding) function σ to ensure that desired model dynamics are obtainable from the system. The desired dynamics in our model are fast response and zero errors in the grid current and the capacitor voltage.

b. Designing a reaching law which warrants that the reaching mode exists.

The controller design requires to have a control law in terms of the switching function (or system states) and system parameters as

$$(s_1, s_2) = f(\sigma, \dot{\sigma}, r_g, L_g, C), \tag{4.1}$$

in order to make the reaching condition of the sliding mode true. By investigating Table 2.2, one may observe that there is a finite set of discrete control inputs. The designer is limited to seven possible control pairs. The finite control set nature of the PUC model complicates the design procedure of the sliding mode controller, which requires that an alternative solution be sought to the control design problem. Hence the controller could be referred to as finite control set sliding mode control (FCS-SMC). The design challenge is to find the control input given in (4.1) as a function of the system states. Moreover, it can be shown that a single sliding function $\sigma = g(x_1, x_2, s_1, s_2)$ engenders the design of the SM controller almost impossible [89]. Therefore, two separate switching functions are designed, one for each error state.

Accordingly, two reaching conditions are derived, one for each switching function. The switching functions are chosen as

$$\begin{aligned} \sigma_1 &= x_1 \\ \sigma_2 &= x_2. \end{aligned} \tag{4.2}$$

Consequently, the following reaching conditions

$$\begin{aligned} \sigma_1 \dot{\sigma_1} &< 0 \\ \sigma_2 \dot{\sigma_2} &< 0, \end{aligned} \tag{4.3}$$

should be validated. In the following subsection, an algorithm is presented for choosing the control inputs to satisfy the conditions in (4.3).

4.2.2 Proposed Control Strategy

In the proposed control method the reaching conditions in (4.3) are put in cost function format as follows

$$\begin{aligned} w_1 &= \sigma_1 \dot{\sigma_1} \\ w_2 &= \sigma_2 \dot{\sigma_2}. \end{aligned} \tag{4.4}$$

Each cost function is evaluated for all the possible control inputs ($i = 1 \dots 7$) listed in Table 2.2. Using (2.6) and (4.2) in (4.4), the cost function of the reaching condition for the grid current defined as

$$w_1^{(i)} = \frac{x_1}{L_g} \left\{ s_1^{(i)} V_{dc} + s_2^{(i)} v_c - r_g x_1 - v_i^* \right\} \tag{4.5}$$

Similarly, using (2.8) and (4.2) in (4.4), the cost function of the reaching condition for the auxiliary capacitor voltage defined as

$$w_2^{(i)} = \frac{-x_2}{C} s_2^{(i)} i_g. \tag{4.6}$$

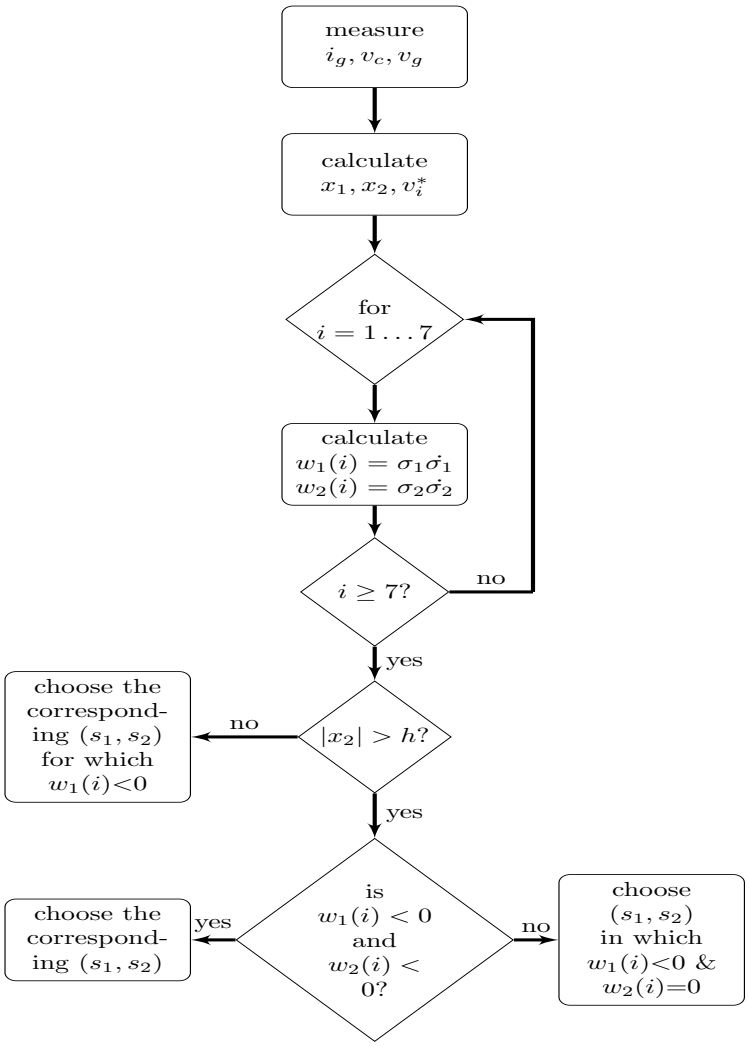


Figure 4.1: Flowchart of FCS-SMC algorithm.

Referring to the flowchart of the control algorithm in figure 4.1, the controller measures the grid voltage and current values, then it calculates the system error states. Then, for the seven possible inputs pairs, the controller evaluates the two cost functions as in (4.5) and (4.6). Figure 4.2 shows the block diagram of the controller. At the end of

the loop, the controller checks if the capacitor voltage error is within some hysteresis band (h) or not. The hysteresis width is a small allowable error value in the capacitor voltage. The hysteresis band for the capacitor voltage is introduced in order to reduce the average switching frequency, as will be shown in Section 4.2.4. If the capacitor voltage is within the hysteresis band then the controller uses the grid current dynamic equation only. Accordingly, the controller investigates the reaching condition for the grid current error, and it picks the control input which makes w_1 in (4.5) negative.

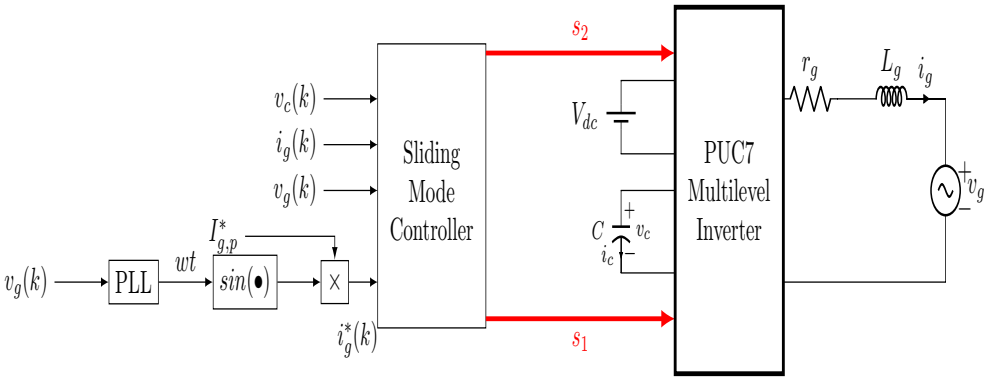


Figure 4.2: Block diagram of the proposed FCS-SMC controller.

On the other hand, if the capacitor voltage is out of the hysteresis band, then the controller investigates both cost functions in (4.5) and (4.6) simultaneously. The controller chooses the corresponding pair in which both cost functions (reaching conditions) have the least negative values to ensure stability of the reaching mode. The choice of least negative values aims at reducing the stress on the converter. If the controller does not find two negative values for $w_1^{(i)}$ and $w_2^{(i)}$ simultaneously, it picks the control input pair where $w_1^{(i)}<0$ and $w_2^{(i)}=0$. Notice that the cost function $w_2^{(i)}$ in (4.6) becomes automatically zero for $i \in \{1,4,7\}$.

4.2.3 Stability

An analytical study of the stability of the proposed SM-controlled system is intractable due to the fact that a mathematical model of the closed loop system is impossible to obtain. The reason for this is that the control variables cannot be expressed explicitly in terms of the system states. Nevertheless, stability can be demonstrated following the procedure described herein. At any sampling instant (k), if we can find at least one pair of control inputs such that the reaching conditions in (4.3) are satisfied, then the stability of the system at that sampling interval is guaranteed. At any sampling time (k), it is required to show that a control pair exists such that for all physically possible values of the states (x_1, x_2, i_g, v_i^*) the reaching conditions are satisfied.

In here, we present one case where $x_1 > 0, x_2 > 0$ and $i_g > 0$. The cost functions (with ignored r_g) at time instant (k) are

$$\begin{aligned} w_1^{(i)}(k) = & \\ & \frac{x_1(k)}{L_g}\left\{s_1^{(i)}(k)V_{dc} + s_2^{(i)}(k)v_c^* + s_2^{(i)}(k)x_2(k) - v_i^*(k)\right\} \\ w_2^{(i)}(k) = & \frac{-x_2(k)}{C}s_2^{(i)}(k)i_g(k), \end{aligned} \tag{4.7}$$

based on these equations we conclude that $w_1(k) < 0$ and $w_2(k) < 0$ if $v_i^*(k) > E$ for the choice of the control pair (0, 1). On the other hand, if $-2E < v_i^*(k) < E$ then the control pair (-1, 1) satisfies the reaching conditions. For $-3E < v_i^* < -2E$ the control pair (-1, 0) leads to $w_1(k) < 0$ and $w_2(k) = 0$. The values of $w_2 = 0$ ($\dot{x_2}(k) = 0$) implies that there will be no change in the capacitor voltage in that sampling interval. However, this situation is likely to change in the following control intervals as the other variables change sign. A similar procedure can be applied to verify that a feasible control pair always exists under all conditions of the other remaining cases.

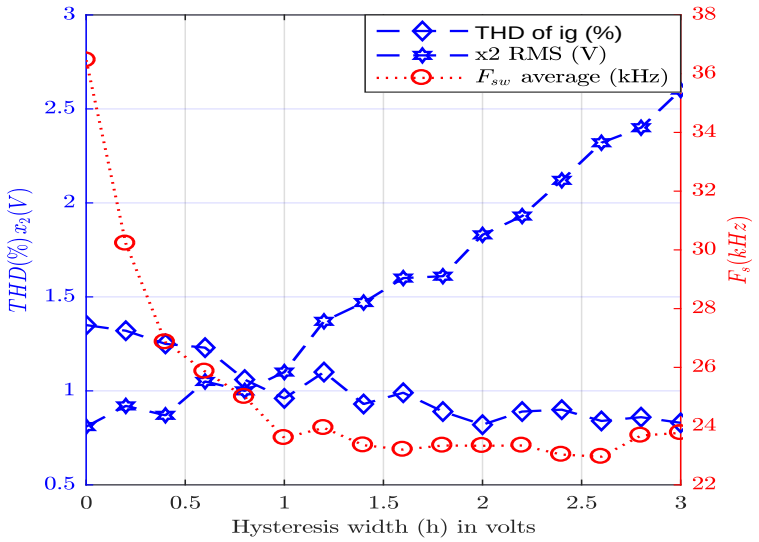


Figure 4.3: Simulation results of PUC performance using FCS-SMC algorithm with varying h.

4.2.4 Hysteresis Width Selection Criteria

One important parameter selection in the design procedure of the proposed SMC is the selection of the capacitor error's hysteresis width (h). The performance of the system for the values of h in the range from 0 to 3 volts is done as shown in figure 4.3. Starting from $h = 0$ and by increasing h, we observe a great reduction in the switching frequency if a small hysteresis band is introduced, this is true up to a certain hysteresis value. After $h \approx 1$ the increase in the THD becomes significant and small reduction in the average switching frequency is observed. The average switching frequency for a switch pair $(S_j, \overline{S}_j)\ j \in \{a,b,c\}$ pairs is calculated as

$$F_{s,\text{av}} = \frac{N_{S_a} + N_{S_b} + N_{S_c}}{T_{\text{total}}} \tag{4.8}$$

where N_{S_a}, N_{S_b} , and N_{S_c} represent the total number of times the three switches (in one leg) switch in a time interval of T_{total}, counting turn ON and turn OFF as two separate switching events. In case of no hysteresis band, the controller gives an equal importance to both errors (similar to MPC algorithm), so if there is a small error in

the capacitor voltage, this will cause the inverter to switch. One may observe the inverse relationship between the average switching frequency and h under allowable capacitor error with slight change in the grid current THD. Observing figure 4.3, the hysteresis band width is set to 1V where this value will be used for the experimental and simulation results.

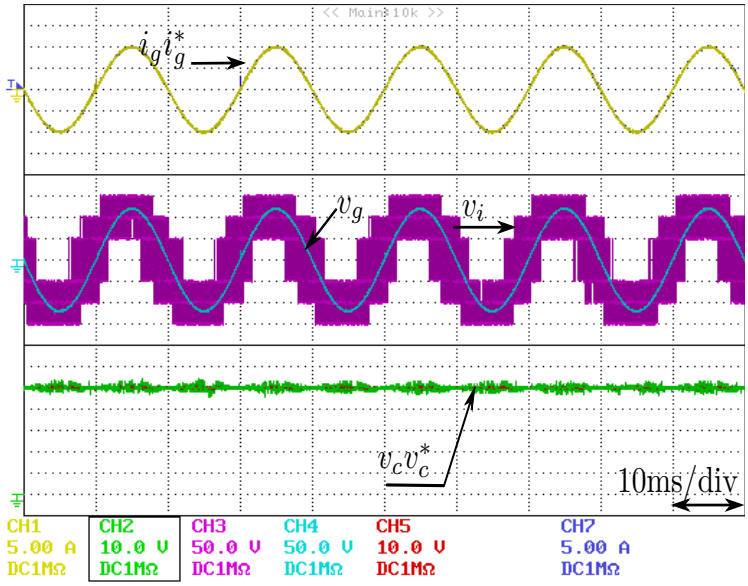


Figure 4.4: Experimental performance of SMC algorithms without hysteresis $h = 0$.

Figure 4.4 depicts the experimental tests of the FCS-SM controller for zero hysteresis band width. From the inverter output voltage waveform it is evident that the FCS-SMC algorithm has high switching frequency for $h = 0$, compared to it's performance when a small hysteresis is introduced (see figure 4.12a in Section 4.4.2). That is owed to the algorithm's selection mechanism, where it chooses any control pair according to the cost functions given in (4.5) and (4.6). In conclusion, it is clear that introducing a hysteresis width for the capacitor voltage error slightly reduces the average switching frequency of the inverter. But the value of h cannot be chosen very large, because this will cause a large error in the capacitor voltage, which eventually deteriorates the inverter's output voltage waveform.

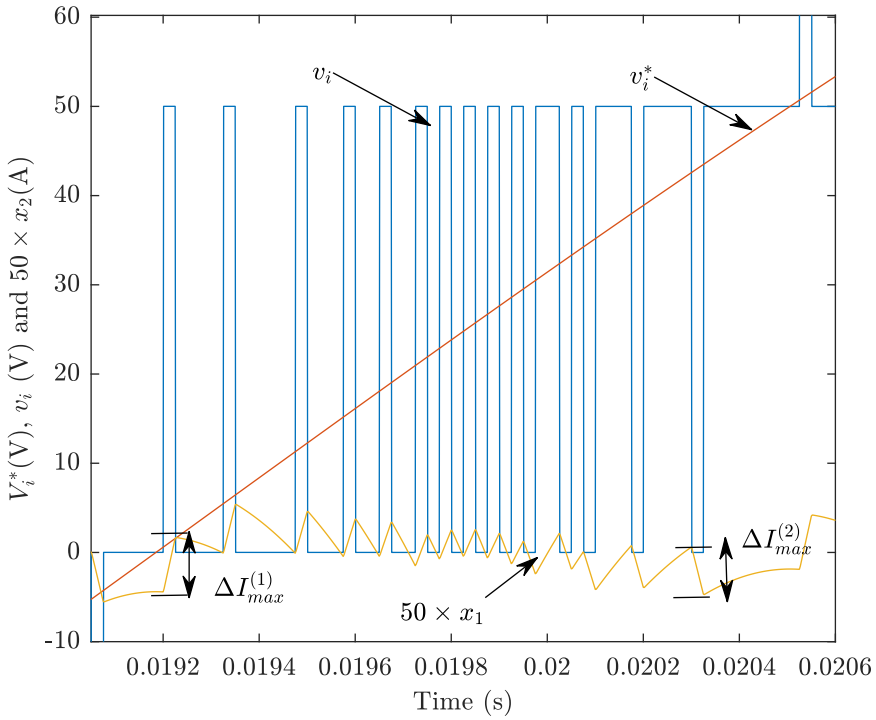


Figure 4.5: Current error ripple, inverter output voltage and inverter voltage reference assuming capacitor voltage error is zero.

4.2.5 Current Ripple Calculation

In this section the high frequency current ripple calculation is made assuming the capacitor voltage is properly controlled. The capacitor voltage error is assumed to be equal to zero ($x_2 = 0$), thus one may replace the capacitor by a fixed dc source which is equal to the capacitor voltage reference. If this is the case, then the controller is required to control the current injected to the grid only according to (4.5). Assuming $r_g = 0$ and replacing v_c by v_c^* in (4.5) then

$$w_1^{(i)} = \frac{x_1}{L_g}\left\{s_1^{(i)} V_{dc} + s_2^{(i)} v_c^* - v_i^*\right\}. \tag{4.9}$$

The above equation contains a time varying function v_i^* where the choice of the control input changes according to the time interval of v_i^*. For simplicity, assume v_i^* is between 0 and E and then assume $x_1 > 0$. The term $s_1^{(i)} V_{dc} + s_2^{(i)} v_c^* - v_i^*$ should be negative,

so the control pair $(s_1^{(i)}, s_2^{(i)})$ is selected to ensure the negativeness of $w_1^{(i)}$. As the algorithm picks the least negative value of $w_1^{(i)}$ then we are minimizing the magnitude of $s_1^{(i)}V_{dc} + s_2^{(i)}v_c^* - v_i^*$. Accordingly the maximum value depends on the difference between the two terms ($s_1^{(i)}V_{dc} + s_2^{(i)}v_c^*$ and v_i^*). Therefore the current ripples at the beginning and at the end of the voltage interval ($0 < v_i^* < E$) are equal and maximum in this interval. This maximum ripple is given as

$$\begin{aligned} \dot{x_1} &= \frac{di_g}{dt} = \frac{1}{L_g}\{s_1V_{dc} + s_2v_c^* - v_i^*\} \\ \Rightarrow \Delta I_{max} &= \frac{T_sE}{L_g}, \end{aligned} \tag{4.10}$$

which has been verified from the simulation results. The same procedure is applied to the voltage interval ($E < v_i^* < 2E$) where the maximum current ripple is given by (4.10), because the voltage difference is also the same in that interval. While for the interval where $v_i^* > 2E$, the maximum current ripple depends on the value v_i^*, where sometimes the current reference is small and other times its larger. Keep in mind that the inverter voltage reference should always be greater than V_g and less than $3E$.

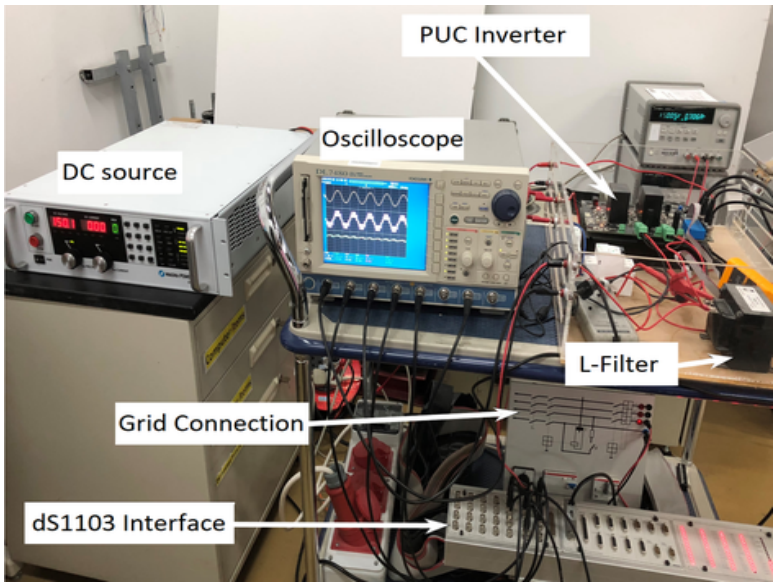


Figure 4.6: Experimental setup.

4.3 Experimental Results

Figure 4.6 shows the experimental setup of the grid-connected 7-level packed U-cell inverter. The control algorithm is implemented using a dSpace dS1103 controller board. The grid voltage is sensed using an LV 25-P voltage sensor and fed to a phase-looked loop (PLL) in order to generate a grid current reference in synchronism with the grid voltage. The capacitor voltage and the grid current are measured using LV 25-P and LEM LA25-P sensors respectively. The input DC voltage is generated from a programmable power supply. Afterwards, the errors (x_1 and x_2) are calculated and used for the FCS-SMC algorithm implementation. Table 4.1 lists the parameters used in the simulations and in the experimental tests.

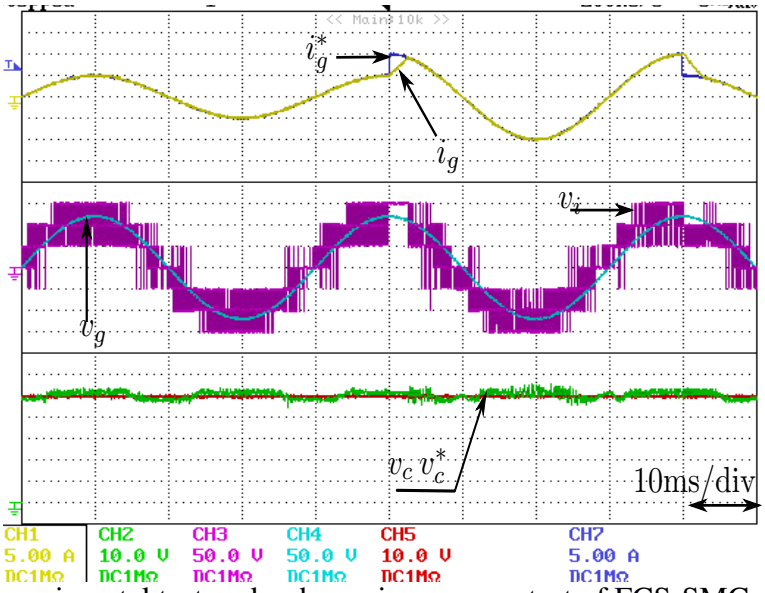


Figure 4.7: Experimental test under dynamic response test of FCS-SMC algorithm for 100% change in the grid reference current.

4.3.1 Dynamic response

The dynamic response of the FCS-SM controller is tested under step change of the grid current reference. Two step changes are applied at the peaks of the sinusoidal reference waveform with 100% increase in the current reference amplitude. Figure. 4.7 shows

the experimental results of the proposed algorithm under dynamic response test, where the controller shows a fast response with stable operation and without overshoot in the current output.

Table 4.1: Simulation and Experimental Parameters.

Parameters	Symbol	Value
Dc voltage source	V_{dc}	150V
Inverter capacitance	C	100 μF
Grid voltage (peak) and frequency	V_g,f_g	120V, 50Hz
Grid inductance and resistance	L_g,r_g	10mH, 0.01Ω
Sampling time	T_s	25μs

4.3.2 Parameters Mismatch Test

Indeed, a parameter mismatch test simulates the realistic usage of the controller, where there is a mismatch between the value used in the controller (measured values) and the actual values in the plant. The experimental results shown in figure 4.8 are obtained under a reduction by 30% in the grid inductance value, which simulates that there is an error in the inductor measurement by 30%. Similarly, figure 4.9 simulates the case when there is a +30% mismatch in the capacitor value. Both results demonstrate the effectiveness of the SM controller in case of parameter mismatches which implies the robustness of the proposed controller against parameter mismatches.

4.3.3 Voltage ride-through capability test

In order to test the voltage ride-through capability, the performance of the proposed FCS-SM controller is investigated under voltage sag and swell. The voltage sag/swell are common grid disturbances, defined as short term reduction/increase in the grid voltage rms values. For the grid voltage sag test, a reduction by 15% of the grid voltage rms is applied to the grid as shown in figure 4.10a. Similarly, an increase by 15% of

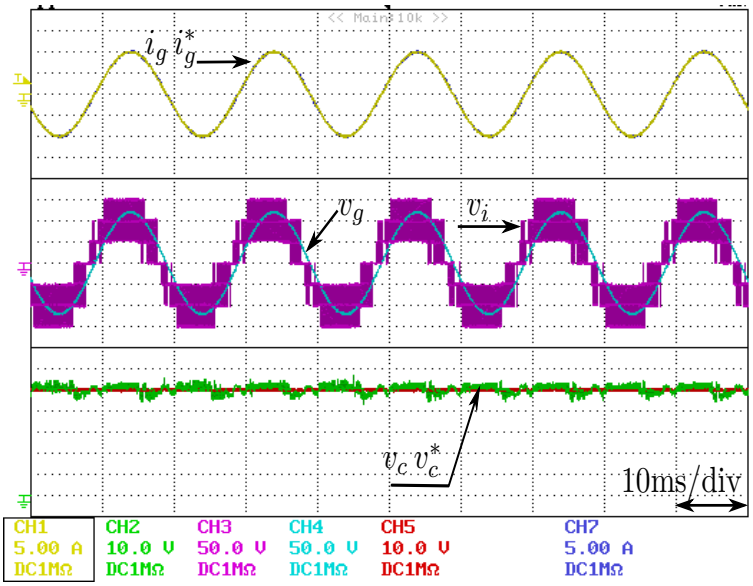


Figure 4.8: Experimental results of FCS-SMC under -30% mismatch in L.

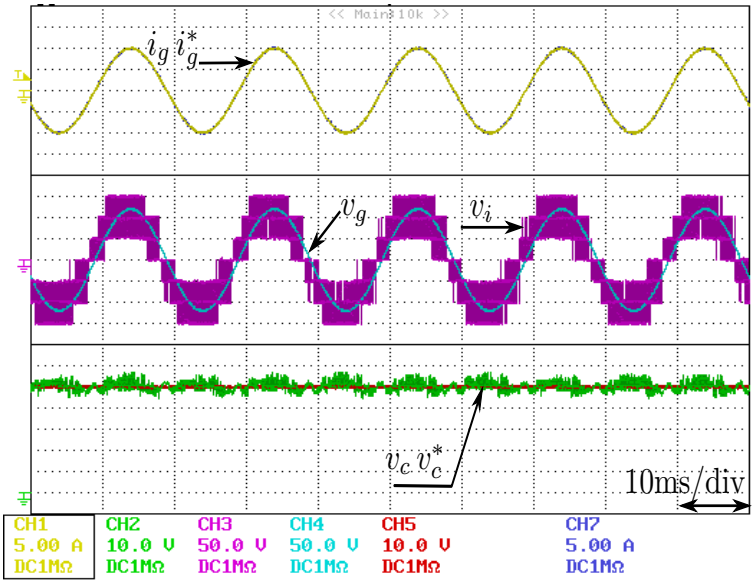
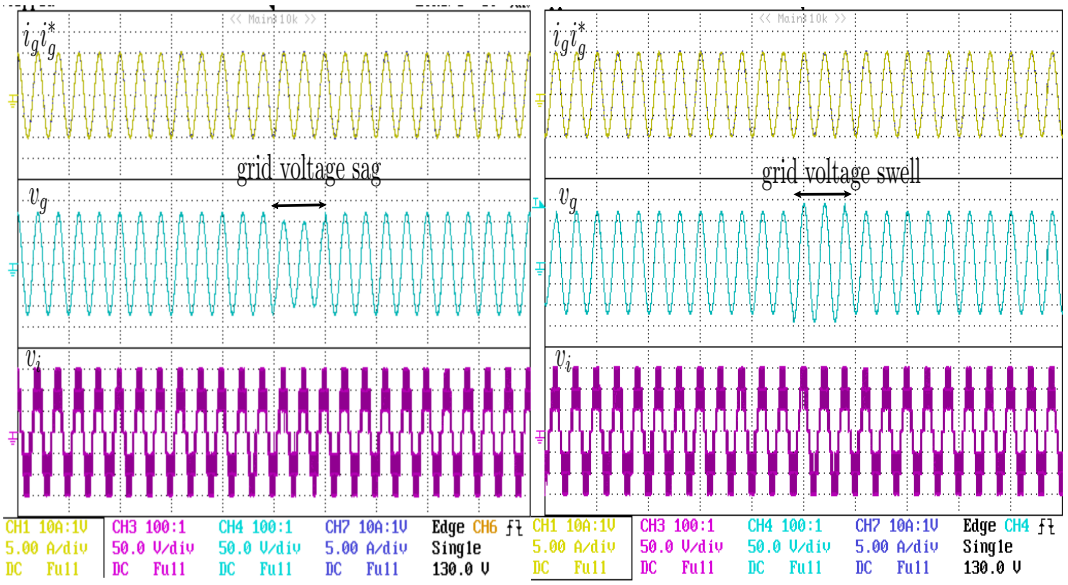


Figure 4.9: Experimental results of FCS-SMC under $+30\%$ mismatch in C.

the grid voltage is applied to the PUC7 inverter as demonstrated in figure 4.10b. Both results demonstrate the effectiveness of the SM controller to inject a pure sinusoidal grid current and generate the required 7-level output voltage.

4.4 Comparison with Conventional FCS-MPC

In this section, a comparison with the work presented in [1] is given, where the conventional FCS-MPC is applied to the PUC7 inverter. The cost function of the



(a) Grid voltage sag. (b) Grid voltage swell.

Figure 4.10: Experimental voltage ride-through capability of FCS-SMC. (top): grid current, (middle): disturbed grid voltage, (bottom): 7-level output voltage.

FCS-MPC is composed of grid current error and weighted capacitor voltage error as

$$g = \lambda \left| \frac{x_2}{\Delta v_{c,\max}} \right| + \left| \frac{x_1}{\Delta i_{g,\max}} \right| \tag{4.11}$$

where $\Delta v_{c,\max} = 2I_g^* T_s / C$ and $\Delta i_{g,\max} = 2V_{dc} T_s / L_g$. The gain associated with the capacitor error was optimally selected as $\lambda = 0.2$.

Table 4.2: Computational load comparison between conventional FCS-MPC vs. the proposed FCS-SMC for one sampling time.

FCS-MPC [1]			FCS-SMC		
required calculation	Mult.	Add.	required calculation	Mult.	Add.
acquisition $v_g(k)$, $i_g(k)$ and $v_c(k)$	-	-	acquisition $v_g(k)$, $i_g(k)$ and $v_c(k)$	-	-
predicting $v_g(k+1)$ and $i_g^*(k+1)$ from (3.7)	2	2	calculating v_i^* from (2.7)	2	3
calculating $v_c(k+1)$ and $i_g(k+1)$ using (4.12)	18^*	28^*	calculating $x_1(k)$, and $x_2(k)$	-	$2\times7=14$
calculating $x_1(k+1)$, and $x_2(k+1)$ from (4.14)	-	$2\times7=14$	calculating w_1 from (4.5)	$2\times7=14^{\ddagger}$	15^*
evaluating (4.11)	$2\times7=14$	$1\times7=7$	calculating w_2 from (4.6)	$1\times4=4^{*\ddagger}$	-
Total	34	51	Total	20	32

(*): The mathematical operations where the control input is equal to zero are eliminated.
(‡) The division by L_g or C is not required.

4.4.1 Computational Load Comparison

In FCS-MPC the states are predicted at the (k+1)st sampling time using system equations in (2.3) and (2.4) as

$$\begin{aligned} v_c(k+1) &= v_c(k) - \frac{T_s}{C} i_g(k) s_2(k) \\ i_g(k+1) &= (1 - r_g T_s / L_g) i_g(k) + \frac{T_s}{L_g} \Big(v_i(k) - v_g(k) \Big). \end{aligned} \tag{4.12}$$

Additionally, the reference current and the grid voltage values are predicted at (k+1) sampling time using first order linear interpolation as

$$\begin{aligned} v_g(k+1) &= \frac{3}{2} v_g(k) - \frac{1}{2} v_g(k-1) \\ i_g^*(k+1) &= \frac{3}{2} i_g^*(k) - \frac{1}{2} i_g^*(k-1). \end{aligned} \tag{4.13}$$

Then the future values of the state errors are calculated according to

$$\begin{aligned} x_1(k+1) &= i_g(k+1) - i_g^*(k+1) \\ x_2(k+1) &= v_c(k+1) - v_c^*, \end{aligned} \tag{4.14}$$

which are used to evaluate the cost function in (4.11).

Table 4.2 summarizes the computational load comparison between FCS-MPC and the proposed FCS-SM controller. It is important to note that the multiplication of any control input with a variable is considered as a sign change, and not as a multiplication. It is clear that the proposed algorithm offers a significant reduction in the required mathematical operations, which increases the algorithm implementation speed. Investigating the control algorithm in figure 4.1 and the computational load table one can observe the simplicity in the implementation of the algorithm compared to FCS-MPC. It is only required to calculate the errors and the inverter voltage reference in order to generate the required control input. On the contrary, FCS-MPC

algorithm is model dependent controller with state estimation and reference voltage prediction (interpolation).

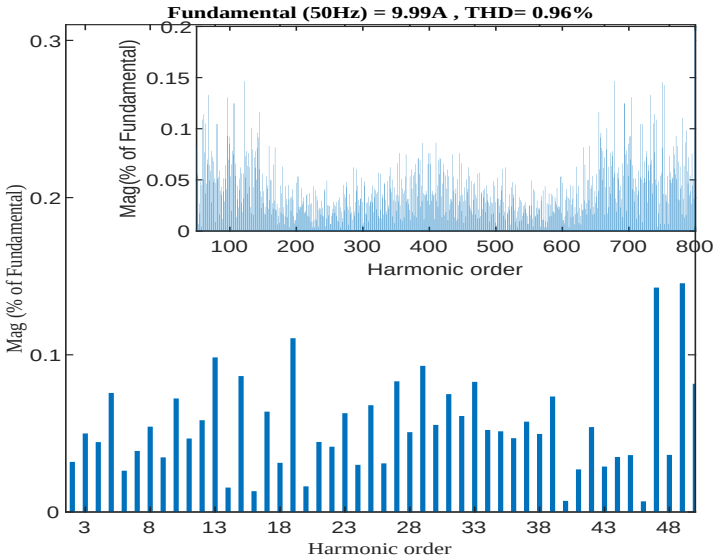
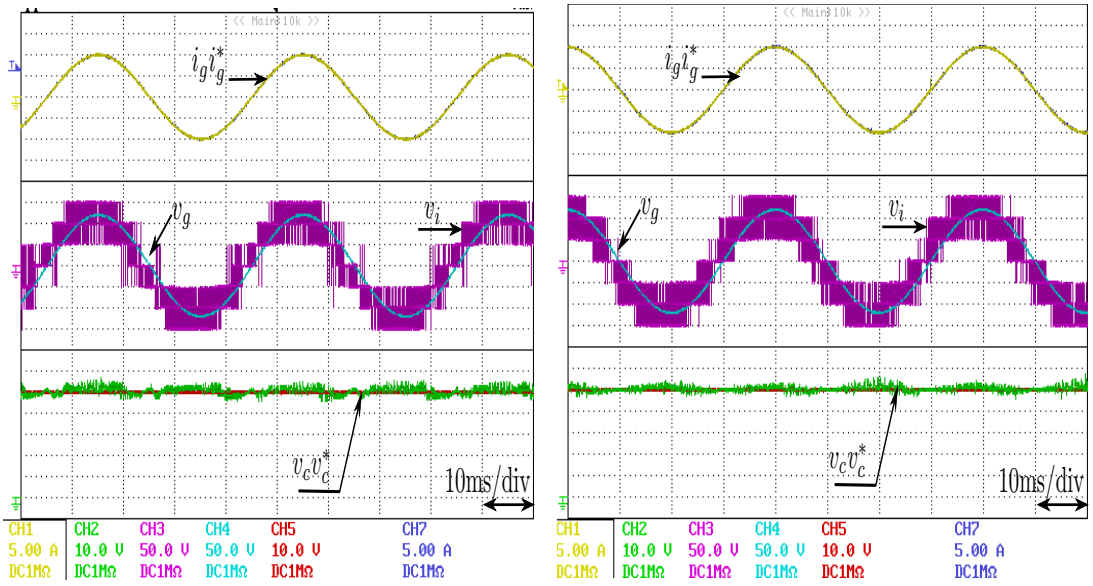


Figure 4.11: Harmonic spectrum of grid current with respect to the fundamental component.

4.4.2 Steady State Performance

Simulation results are compared for the proposed FCS-SMC algorithm versus the conventional FCS-MPC. In the comparisons, the grid current reference is set to 10A peak, and a summary of the comparative test is listed in Table 4.3. The THD of the proposed method for 10A peak grid current reference is given in figure 4.11. The steady state experimental results are given in figure 4.12 where the proposed FCS-SMC algorithm demonstrates similar performance to the FCS-MPC control method. For both algorithms the grid current is properly controlled. One may notice that there are a larger number of level changes in the inverter output voltage for FCS-MPC algorithm. Indeed this implies that there is a higher switching frequency and accordingly slightly lower THD.



(a) FCS-SMC. (b) FCS-MPC.

Figure 4.12: Experimental results during active power injection to the grid (10A peak) at steady state. (top): grid current and it's reference, (middle): inverter output voltage and grid voltage, (bottom): capacitor voltage and it's reference.

On the other hand, the capacitor voltage error in FCS-SMC algorithm is slightly lower than MPC and reaching up to the maximum allowable value of h. The slight increase in the hysteresis width is desirable in order to reduce the switching frequency (which implies a slight increase in the current THD).

Table 4.3: Comparison table: SM control algorithm vs Classical MPC.

Parameter	SMC $h = 1V$	MPC $\lambda = 0.2$
THD of $i_g(\%)$	0.96	0.75
$F_{s,av}$ (kHz)	23.60	25.85
x_2 RMS (V)	1.1	1.28

Notice that using FCS-SMC method the error in the capacitor is controlled by varying the hysteresis width (h) of the capacitor voltage error. So the capacitor maximum error amplitude is limited to the hysteresis width, while in MPC the error in the capacitor voltage cannot be directly related to the gain associated with the capacitor error in the cost function. In conventional MPC, the choice of the gain λ does not give any idea

about the error of the capacitor voltage. This is another advantage to be added to the proposed SMC algorithm.

4.5 Conclusions

In this chapter, a simple and effective sliding mode controller design is presented and applied to a 7-level PUC inverter. The proposed controller takes the advantage of the sliding mode control theory to overcome the complex nature of the PUC model. The control set is chosen according to a cost function derived from the reaching condition of SMC. The main advantages of the proposed SMC method are: 1) simplicity in design and implementation; 2) Gain tuning is not required; 3) Low computational complexity; 4) Introduction of the hysteresis bandwidth for the capacitor voltage allows reduction in the average switching frequency and expresses direct relation between the acceptable capacitor error and the hysteresis bandwidth. Simulation and experimental results were presented to prove the effectiveness of the proposed algorithm in terms of dynamic performances, harmonic distortion, and robustness against disturbances and parameter mismatches.

Chapter 5

A REDUCED SENSOR LYAPUNOV-BASED MODEL PREDICTIVE CONTROL DESIGN FOR A PUC7 DUAL OUTPUT RECTIFIER

5.1 Introduction

The work presented in this chapter is considered as an application of the Lyapunov-based MPC controller in [56] to the PUC rectifier with a dual output. The proposed controller is similar to the conventional model predictive controller except for the fact that the cost function is derived from a stability point-of-view. The controller picks the control input which corresponds to the minimum value of the Lyapunov cost function. Though the cost function includes three control variables (two capacitor voltages and source current), yet gain tuning is not required as in conventional MPC and it is simple in implementation. Additionally, the proposed controller doesn't require load current sensors; instead, the controller predicts the loads measurement based on the mathematical model of the PUC rectifier.

In the following section the mathematical model of the PUC7 converter is presented in Section 5.2. In Section 5.3, the controller design procedure is introduced including the design of the Lyapunov-based MPC algorithm. The simulations and the experimental results are given in Section 5.4 with conclusions given in Section 5.5.

5.2 Mathematical Model of the PUC7 Rectifier

A dual output PUC7 boost rectifier is shown in figure 5.1. The rectifier is connected to the source through a simple L-filter L_s, with internal resistance r_s. The converter's loads are resistors in parallel with filtering capacitors. The upper load voltage with nominal resistor value of R_1 is required to be three times the lower load which has the nominal resistance value R_2, and reference voltage of E. Thus, the converter is expected to produce a seven-level output voltage at it's input ($\{\pm 3E \pm 2E \pm E\}$ and $\{0\}$). Each load is connected to a parallel capacitor (C_1, C_2) with output voltages v_{o1} and v_{o2}, respectively.

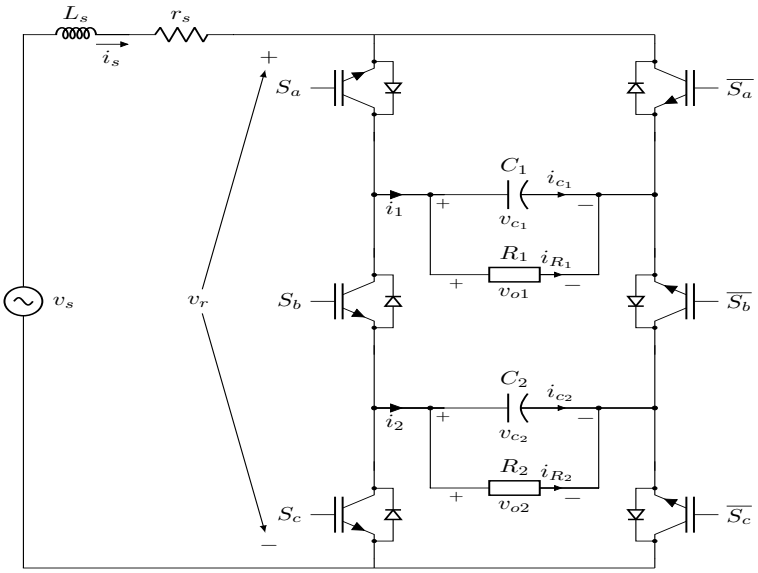


Figure 5.1: A dual output grid-connected PUC7 converter.

Each switch S_k for $k \in \{a,b,c\}$ it has a state of $s_k = 1$ when it is closed and $s_k = 0$ when it is open. Following this definition, the control input switching functions of the converter can be defined as

$$\begin{aligned} s_1 &= s_a - s_b \\ s_2 &= s_b - s_c. \end{aligned} \tag{5.1}$$

Table 5.1: PUC7 Switching States And Terminal Voltages.

index (l)	s_1	s_2	s_a	s_b	s_c	v_r	$v_r\big\vert_{\substack{v_{c_1}=3E \\ v_{c_2}=E}}$
1	+1	0	1	0	0	v_{c_1}	$3E$
2	+1	−1	1	0	1	$v_{c_1}-v_{c_2}$	$2E$
3	0	+1	1	1	0	v_{c_2}	E
4	0	0	1	1	1	0	0
	0	0	0	0	0	0	0
5	0	−1	0	0	1	$-v_{c_2}$	$-E$
6	−1	1	0	1	0	$-v_{c_1}+v_{c_2}$	$-2E$
7	−1	0	0	1	1	$-v_{c_1}$	$-3E$

Considering Table 5.1 and figure 5.1, the current equations of the load side are

$$i_1 = s_1 i_s = i_{c_1} + i_{o1}, \quad i_2 = s_2 i_s = i_{c_2} + i_{o2}, \tag{5.2}$$

with capacitor dynamics described as

$$C_1 \frac{dv_{c_1}}{dt} = s_1 i_s - i_{o1}, \quad C_2 \frac{dv_{c_2}}{dt} = s_2 i_s - i_{o2}. \tag{5.3}$$

The PUC7 rectifier output voltage is given as

$$v_r = s_1 v_{c_1} + s_2 v_{c_2}, \tag{5.4}$$

which is a 7-level input voltage waveform. However the source current dynamic is given as

$$\frac{di_s}{dt} = -\frac{r_s}{L_s} i_s + \frac{1}{L_s}\left(v_s - v_r\right). \tag{5.5}$$

As the function of the converter is to supply the loads with the necessary power taken from the source, the converter is required to operate in order to maintain the following: 1) control the load voltages v_{o1} v_{o2} to their reference values $3E$ and E, respectively. 2) To draw a sinusoidal source current which is in phase with the source voltage; which implies a unity power factor operation. Consequently, the converter

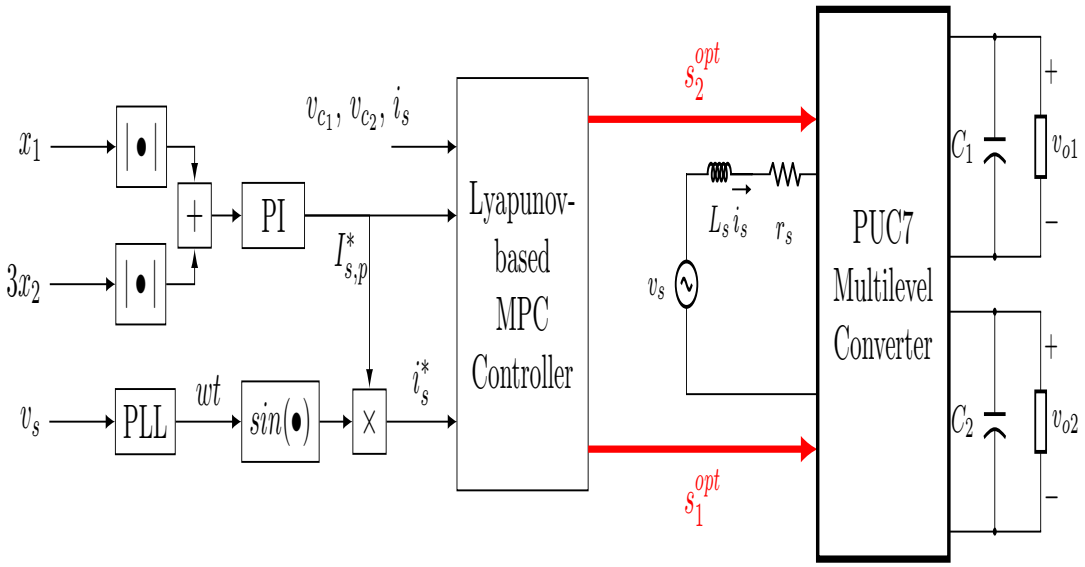


Figure 5.2: Lyapunov-based FCS-MPC block diagram.

should be controlled in order to maintain these objectives. For that, the following error definitions are given:

$$x_1 = v_{c_1} - v^*_{c_1}, \tag{5.6}$$

and

$$x_2 = v_{c_2} - v^*_{c_2} \tag{5.7}$$

which represent the load voltage errors. Utilizing (5.3) we can find the derivatives of the load voltage errors as

$$\dot{x_1} = \frac{1}{C_1}(s_1 i_s - i_{o1}) \tag{5.8}$$

and

$$\dot{x_2} = \frac{1}{C_2}(s_2 i_s - i_{o2})\,. \tag{5.9}$$

Similarly, the source current error is defined as

$$x_3 = i_s - i^*_s, \tag{5.10}$$

where i^*_s represents the sinusoidal reference current of the source. Using (5.5), the

source current error derivative is given as

$$\begin{aligned} \dot{x_3} &= \frac{di_s}{dt} - \frac{di_s^*}{dt} \\ &= -\frac{r_s}{L_s} i_s + \frac{1}{L_s}(v_s - v_r) - \frac{di_s^*}{dt}, \end{aligned} \tag{5.11}$$

which can be simplified to the following form

$$\dot{x_3} = \frac{1}{L_s}(v_{in}^* - v_r). \tag{5.12}$$

In (5.12) v_{in}^* represents the rectifier reference input voltage assuming the reference current i_s^* passes through the source inductance, with measured source voltage. The reference converter voltage is calculated as

$$v_{in}^* = v_s - L_s \frac{di_s^*}{dt} - r_s i_s^* \tag{5.13}$$

In the following the design of the controller is presented.

5.3 Controller Design

The operating principle of the controller is similar to the conventional FCS-MPC controller presented in [1, 33] except for the fact that a different cost function is utilized in this MPC controller. The cost function is derived based on Lyapunov control theory [88], where the controlled system (the PUC7 converter) is governed from a stability point-of-view. The block diagram of the overall controller is given in figure 5.2. As the aim of the rectifier is to control the dual output load voltages and the source current, the output voltage errors are calculated as x_1 and x_2, where a ratio of 3 is associated with x_2 to ensure error ratio balance between different errors. Then the sum of the absolute values of x_1 and $3x_2$ is directed to the input of the proportional

integral controller to produce the reference source current peak $I^*_{s,p}$ as

$$I^*_{s,p} = k_p\, e + k_i \int e\, dt, \tag{5.14}$$

where $e = (|x_1| + 3|x_2|)$ represents the total input error to the PI controller. Simultaneously, using a phase-looked loop (PLL) the phase of the source voltage v_s is found; which is directed to a sine function with output multiplied by the peak reference current from the PI controller resulting in the source current reference i^*_s. For unity power factor operation, the source voltage and the generated reference current are kept in phase. Lyapunov-based MPC algorithm requires the value of the source current reference i^*_s, the measured source voltage v_s and the measured load voltages v_{C_1} and v_{C_2}. Basically, the controller evaluates a cost function for all the possible input pairs and it picks the control input pair which corresponds to the minimum value of the cost function. In the following sections, a detailed design procedure is given.

5.3.1 Discrete Model and System States Prediction

Similar to the conventional MPC-based controller, the discrete-time model of the PUC7 is obtained. For a fixed sampling period T_s, the first order forward Euler approximation of (5.3) and (5.5) are

$$\begin{aligned} v_{c_1}(k+1) &= v_{c_1}(k) + \frac{T_s}{C_1}\Big(s_1(k) i_s(k) - i_{o1}(k)\Big) \\ v_{c_2}(k+1) &= v_{c_2}(k) + \frac{T_s}{C_2}\Big(s_2(k) i_s(k) - i_{o2}(k)\Big) \\ i_s(k+1) &= (1 - r_s T_s/L_s)\, i_s(k) + \frac{T_s}{L_s}\Big(v_s(k) - v_r(k)\Big), \end{aligned} \tag{5.15}$$

where

$$v_r(k) = s_1(k) v_{c_1}(k) + s_2(k) v_{c_2}(k). \tag{5.16}$$

The predicted values derived in this section are used in the algorithm. The source voltage, the current reference value and the converter reference voltage are predicted at (k+1) sampling time as follows

$$\begin{aligned} v_s(k+1) &= \frac{3}{2}v_s(k) - \frac{1}{2}v_s(k-1) \\ i_s^*(k+1) &= \frac{3}{2}i_s^*(k) - \frac{1}{2}i_s^*(k-1), \end{aligned} \tag{5.17}$$

and

$$v_{in}^*(k+1) = v_s(k+1) - \frac{L_s}{T_s}\{i_s^*(k+1) - i_s^*(k)\} - r_s i_s^*(k+1). \tag{5.18}$$

Furthermore, the output of (5.14) at (k+1) sampling time is

$$I_{s,p}^*(k+1) = k_p e(k+1) + k_i \int_0^{(k+1)T_s} e(t)dt, \tag{5.19}$$

and sampling time (k) is

$$I_{s,p}^*(k) = k_p e(k) + k_i \int_0^{kT_s} e(t)dt, \tag{5.20}$$

subtracting(5.20) from (5.19) and simplifying gives,

$$I_{s,p}^*(k) = I_{s,p}^*(k-1) + K_1 e(k) + K_2 e(k-1), \tag{5.21}$$

where $K_1 = k_p + k_i T_s/2$ and $K_2 = k_i T_s/2 - k_p$

5.3.2 Cost Function Design

As the main contribution in this chapter is the design of the cost function which is derived based on Lyapunov control method, a brief theory explanation is given here. Lyapunov direct method of stability states that if a positive definite function (e.g. $V(\mathbf{x})$) which is defined in terms of the system states ($\mathbf{x}$) exists, then the stability of the controlled system is guaranteed if the following conditions hold

1) $V(\mathbf{x})$ is positive definite.

2) $\dot{V}(\mathbf{x})$ is negative definite.

3) $V(\mathbf{x})$ goes to ∞ as $\|\mathbf{x}\| \to \infty$.

Because the Lyapunov function is an "energy-like" function, an increase in the function implies growth in the states, whereas a reduction in it implies a reduction in the states value. While the states settle at the origin $\mathbf{x} = 0$ when $V(\mathbf{x})$ becomes zero.

In this research work, the following Lyapunov function is used

$$V(\mathbf{x}) = \frac{\alpha_1}{2}x_1^2 + \frac{\alpha_2}{2}x_2^2 + \frac{\alpha_3}{2}x_3^2. \tag{5.22}$$

The gains α_k for $k \in \{1,2,3\}$ are design parameters to be chosen as real and positive numbers. Notice that $\mathbf{x} = [x_1\, x_2\, x_3]^T$ is the vector of the error states. As the function in (5.22) is positive definite, then by making $\dot{V}(\mathbf{x}) < 0$ for all values of $\mathbf{x}$, the stability of the controlled system represented by (5.3) and (5.5) is guaranteed [56]. Taking the derivative of (5.22) gives

$$\dot{V}(\mathbf{x}) = \alpha_1 x_1 \dot{x}_1 + \alpha_2 x_2 \dot{x}_2 + \alpha_3 x_3 \dot{x}_3. \tag{5.23}$$

Substituting equation (5.8), (5.9) and (5.12) in (5.23) gives

$$\begin{aligned}\dot{V}(\mathbf{x}) = &\frac{\alpha_1 x_1}{C_1}\left(s_1 i_s - i_{o1}\right) + \frac{\alpha_2 x_2}{C_2}\left(s_2 i_s - i_{o2}\right) \\ &+ \frac{\alpha_3 x_3}{L_s}\left(v_{in}^* - v_r\right).\end{aligned} \tag{5.24}$$

Equation (5.10) is used to substitute for the value of the measured source current i_s in terms of its reference value and the current error. Similarly, the value of v_r is maintained from (5.4), whereas the capacitor voltages are replaced by their corresponding values in (5.6) and (5.7), respectively. After these substitutions,

equation (5.24) can be written as

$$\begin{aligned}\dot{V}(\mathbf{x}) = \frac{\alpha_1 x_1}{C_1}\{s_1(x_3+i_s^*)-i_{o1}\}+\frac{\alpha_2 x_2}{C_2}\{s_2(x_3+i_s^*)-i_{o2}\}\\ +\frac{\alpha_3 x_3}{L_s}\{v_{in}^*-s_1(x_1+v_{c_1}^*)-s_2(x_2+v_{c_2}^*)\},\end{aligned} \tag{5.25}$$

which simplifies to

$$\begin{aligned}\dot{V}(\mathbf{x}) = s_1x_1x_3\{\frac{\alpha_1}{C_1}-\frac{\alpha_3}{L_s}\}+s_2x_2x_3\{\frac{\alpha_2}{C_2}-\frac{\alpha_3}{L_s}\}\\ +\frac{\alpha_1 x_1}{C_1}\{s_1i_s^*-i_{o1}\}+\frac{\alpha_2 x_2}{C_2}\{s_2i_s^*)-i_{o2}\}\\ +\frac{\alpha_3 x_3}{L_s}\{v_{in}^*-(s_1v_{c_1}^*+s_2v_{c_2}^*)\}.\end{aligned} \tag{5.26}$$

The following choices are made in order to eliminate x_1x_3 and x_2x_3 terms [56]

$$\begin{aligned}\alpha_1 &= \frac{C_1\alpha_3}{L_s}\\ \alpha_2 &= \frac{C_2\alpha_3}{L_s},\end{aligned} \tag{5.27}$$

where α_3 is chosen to be any arbitrary positive number. In the following sections it will be shown that the choice of α_3 has no influence on the controller performance as long as it's positive number. Substituting(5.27) in (5.26) we get

$$\begin{aligned}\dot{V}(\mathbf{x}) = \frac{\alpha_3}{L_s}\Big(x_1\{s_1i_s^*-i_{o1}\}+x_2\{s_2i_s^*-i_{o2}\}\\ +x_3\{v_{in}^*-(s_1v_{c_1}^*+s_2v_{c_2}^*)\}\Big).\end{aligned} \tag{5.28}$$

Notice that the choice of the control input in the algorithm should maintain equation (5.28) negative in order to ensure the stability of the controlled system.

5.3.3 Lyapunov-based MPC Algorithm

Lyapunov-based MPC controller shown in figure5.2 replaces the cost function of the conventional model predictive controller by the cost function in (5.28). The controller picks the control input pair $(s_1(k), s_2(k))$ which corresponds to the minimum value of

Algorithm 2 Lyapunov-based MPC algorithm for PUC7 rectifier.

1: Sampling $v_s(k), i_s(k), v_{c_1}(k), v_{c_2}(k)$.
2: Estimate the currents' output using (5.30).
3: Calculate (5.17) and (5.18).
4: **for** $l = 1 \dots 7$ **do**
5: Calculate (5.31), (5.32) and (5.33).
6: Evaluate (5.29).
7: **return** minimum $\dot{V}_{\mathbf{x}}(k+1)$
8: Choose the switching pair for which $\dot{V}_x(k+1)$ is minimum.

the Lyapunov function. The minimum value of the cost function ensures that $\dot{V}_{\mathbf{x}}(k+1)$ is negative which implies that the stability of the system is guaranteed. It is important to point out that from now on, the cost function of the proposed MPC and the derivative of the Lyapunov cost function are interchangeably used. The cost function of the Lyapunov-based MPC evaluated at k+1 sampling time is

$$\begin{aligned}\dot{V}_{\mathbf{x}}(k+1) = \frac{\alpha_3}{L_s}\Big(& x_1(k+1)\{s_1(k)i_s^*(k+1) - i_{o1}(k+1)\} \\ & + x_2(k+1)\{s_2(k)i_s^*(k+1) - i_{o2}(k+1)\} \\ & + x_3(k+1)\{v_{in}^*(k+1) - (s_1(k)v_{c_1}^* + s_2(k)v_{c_2}^*)\}\Big),\end{aligned} \tag{5.29}$$

As the values of $i_{o1}(k+1)$ and $i_{o2}(k+1)$ are not available at the sampling instant k, and in order to avoid using current sensors for the load currents, the estimated values of the load currents are calculated from (5.15) as

$$\begin{aligned} i_{o1}(k+1) \approx \hat{i}_{o1}(k) = s_1(k-1)i_s(k) - \frac{C_1}{T_s}\Big(v_{c_1}(k) - v_{c_1}(k-1)\Big) \\ i_{o2}(k+1) \approx \hat{i}_{o2}(k) = s_2(k-1)i_s(k) - \frac{C_2}{T_s}\Big(v_{c_2}(k) - v_{c_2}(k-1)\Big). \end{aligned} \tag{5.30}$$

Using (5.15) the value of the first capacitor voltage error at the (k+1) sampling time is calculated as

$$\begin{aligned} x_1(k+1) &= v_{c_1}(k+1) - v_{c_1}^* \\ &= x_1(k) + \frac{T_s}{C_1}\Big(s_1(k)i_s(k) - \hat{i}_{o1}(k)\Big). \end{aligned} \tag{5.31}$$

The second capacitor voltage error at (k+1) is

$$\begin{aligned} x_2(k+1) &= v_{c_2}(k+1) - v_{c_2}^* \\ &= x_2(k) + \frac{T_s}{C_2}\Big(s_2(k)i_s(k) - \hat{i}_{o2}(k)\Big). \end{aligned} \tag{5.32}$$

Whereas the source current error at the next sampling instant is found using (5.15) as

$$\begin{aligned} x_3(k+1) &= i_s(k+1) - i_s^*(k+1) \\ &= (1 - \{r_s T_s\}/L_s)\, x_3(k) + \frac{T_s}{L_s}\Big(v_s(k) - v_r(k)\Big) \\ &\quad - i_s^*(k+1) \end{aligned} \tag{5.33}$$

The control algorithm is given in Algorithm 2, where the states are measured at sampling instant k and the future values are predicted according to (5.17).

Table 5.2: Simulation and Experimental Parameters.

Parameters	Symbol	Value
Load reference voltages	$v_{c_1}^*$, $v_{c_2}^*$	210 V, 70 V
Inverter capacitances	$C_1 = C_2$	300 μF
Source voltage (peak) and frequency	$V_{s,p}$, f_s	100 V, 50 Hz
Source inductance	L_s	10 mH,
Source resistance	r_s	0.01 Ω
Sampling time	T_s	20 μs
PI controller gains	k_p and k_i	2 and 0.2
Current gain	α	1

5.4 Simulation and Experimental Results

Table 5.2 lists the parameters used for both simulation and experimental tests. Simulations were done using Matlab/SPS toolbox. The control algorithm is embedded into a dSpace dS1103 controller board for experimental verification with sampling time of 20 μs. LEM LV 25-P voltage sensor and LEM LA 25-P current sensor are used to measure the voltages and the current values, respectively. During different tests, different values of load resistance's are used in order to show the

performance of the converter over a wide range of load values

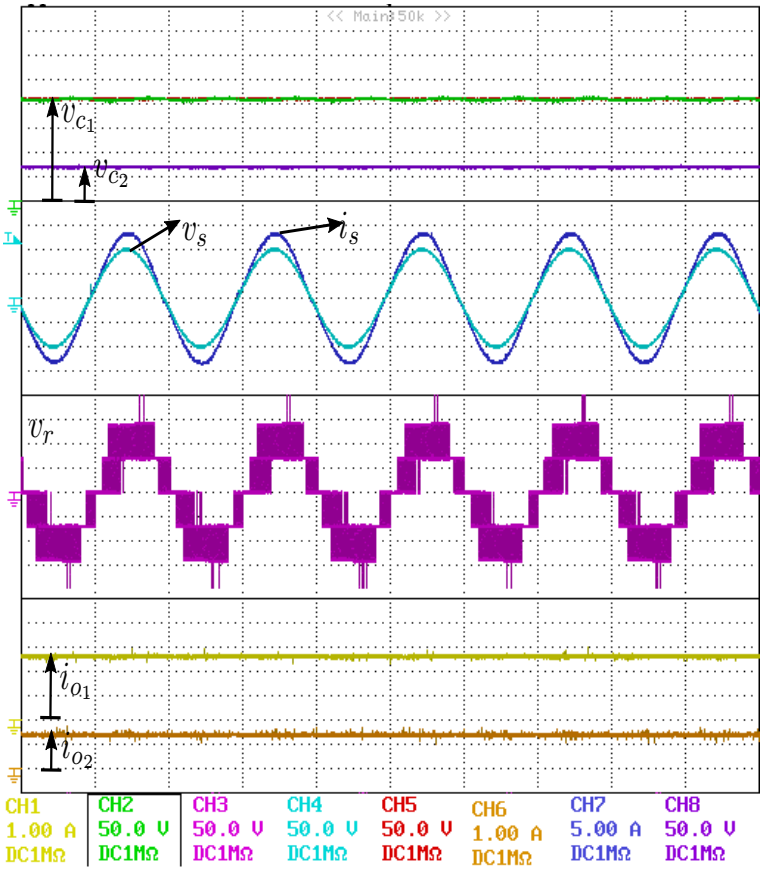


Figure 5.3: Experimental results of PUC7 rectifier performance during steady state. The load resistors are $R_1 = 80\Omega$ and $R_2 = 50\Omega$.

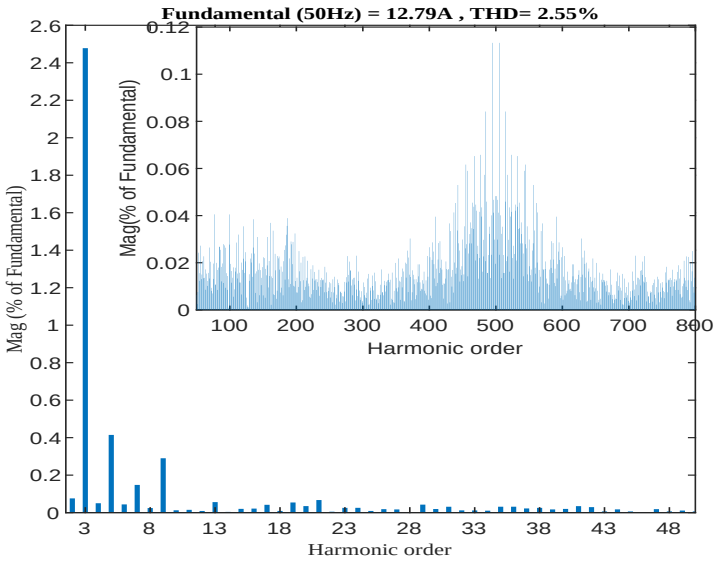


Figure 5.4: Harmonic spectrum of the source current.

5.4.1 Steady State Test

Experimental results for steady state operation are given in figure 5.3 for total power of 650 W absorbed from the source. From the figure it is clear that the capacitor voltages are controlled to their reference voltages, with dc load current values of 2.6 A and 1.4 A for the first and the second load, respectively. Moreover, one can see that the source current is in phase with the source voltage with peak value of 13 A. The harmonic spectrum shown in figure 5.4 is obtained from the simulation with total harmonic distortion value of 2.55%. The converter seven level outputs are clearly obtained as shown in the figure, though we have a few step jumps for the levels of $3E$ and $-3E$ which is explained as being due to the small amount of power supplied to the loads in this test. If higher power values are supplied to the loads, the levels will be more visible.

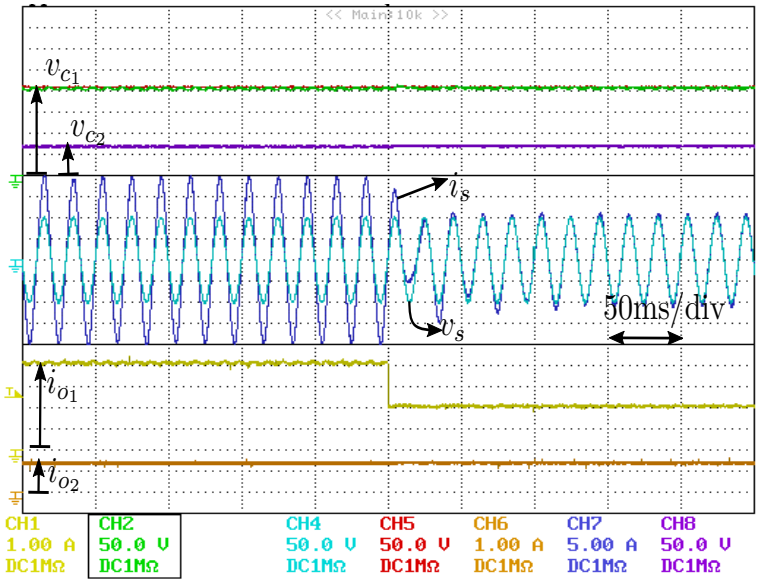


Figure 5.5: Experimental results of PUC7 rectifier performance for step change in the first load (R_1 changed from 100 to 50 Ω, and $R_2 = 50\Omega$ unchanged).

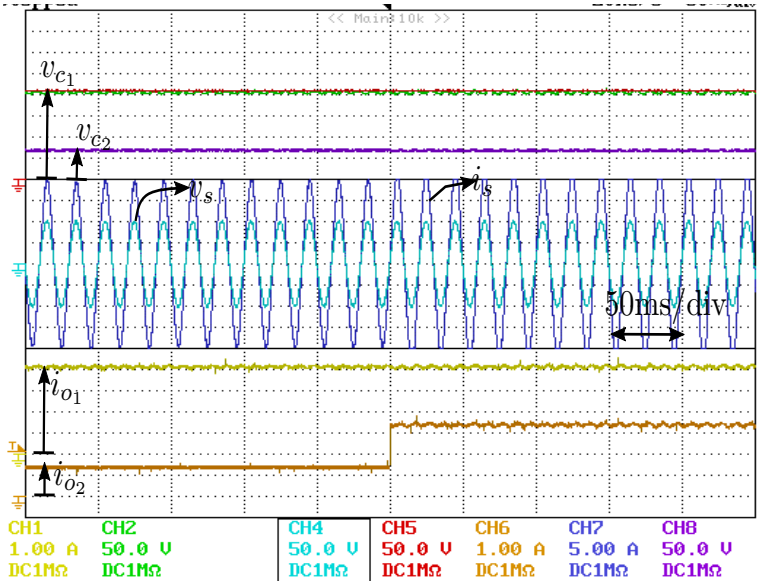


Figure 5.6: Experimental results of PUC7 rectifier performance for step change in the second load (R_2 changed from 20 to 50 Ω, and $R_1 = 50\Omega$ unchanged).

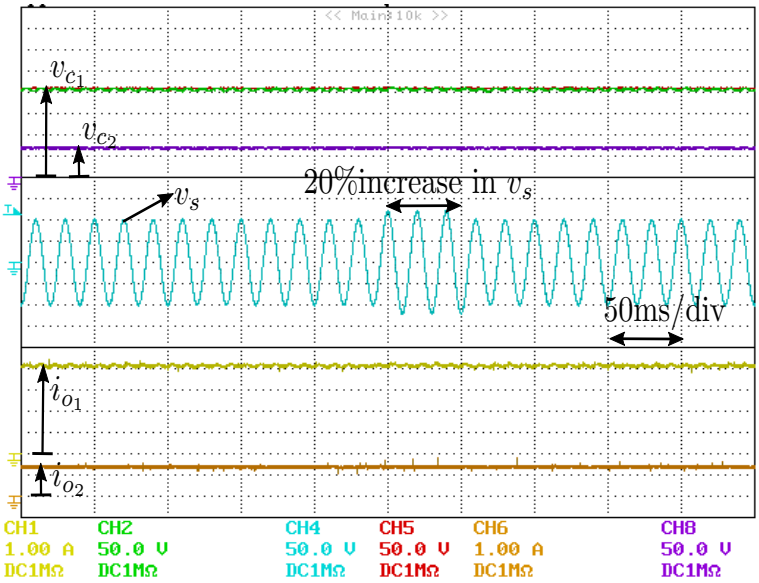


Figure 5.7: Experimental results during supply variation test for PUC7 rectifier ($R_1 = R_2 = 50\Omega$).

5.4.2 Dynamic Performance Test

The dynamic performance test is applied for the loads and source voltage changes. First, a test is set for 50% step change in the first load as in figure 5.5. The resistor value is changed from 100 Ω to 50 Ω, while R_2 is unchanged during the test with value of 50 Ω. The first and the second load power were P_1 = 441 W and P_2 = 98 W, with total power change from 539 W to 980 W, approximately. Notice that the controller

is able to properly control the source current during the transient period of the load change, and one may observe the good behavior of the source current during and after the load change.

The second test is performed by fixing the first load resistance value to 50 Ω, while the second load resistor is changed from 20 Ω to 50 Ω. In this test a reduction in the total power consumed from the source is applied to the converter as it can be seen from the source current shown in figure 5.6.

As the source voltage is assumed to be measured in the controller, variation in it's value is very common in the grid-connected application. For that, an increase by 20% in the nominal source voltage peak is applied to the converter where the load resistances are fixed to 50 Ω. The experimental results in figure 5.7 shows the good response of the controller during the whole test, where the total power absorbed by the loads is approximately 980 W, and the output voltages are controlled to their references value.

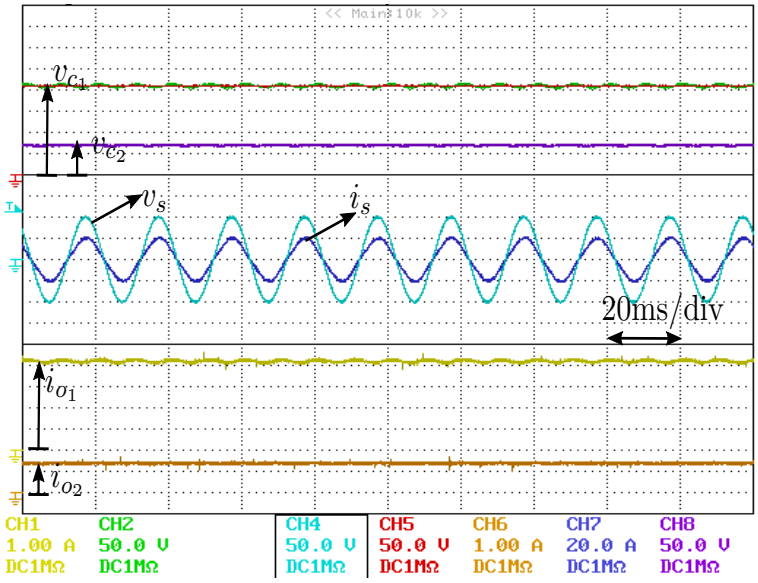


Figure 5.8: Experimental results during +30% mismatch in source inductance value L_s ($R_1 = R_2 = 50\Omega$).

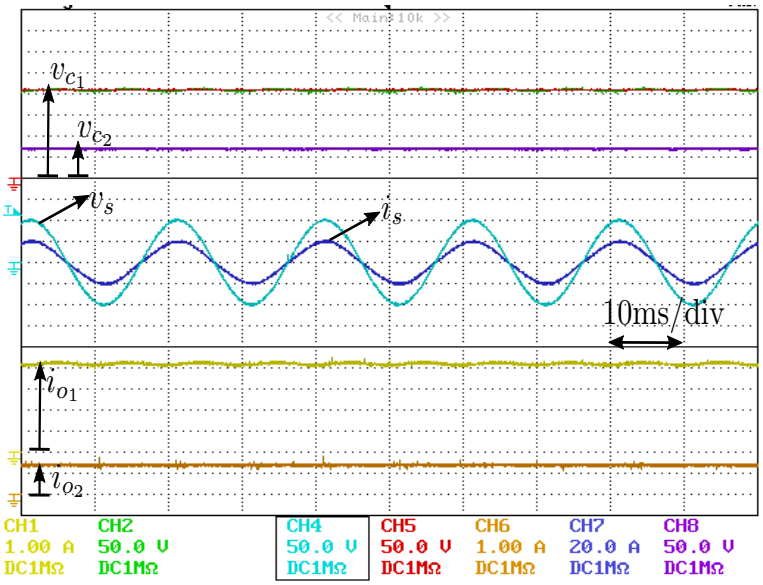


Figure 5.9: Experimental results during $+30\%$ mismatch in load capacitances values C_1 and C_2 ($R_1 = R_2 = 50\Omega$).

5.4.3 Parameter Mismatch

As the parameter values of capacitors and the inductor may vary due to heat, measurement inaccuracy, and time, it is required to test the influence of parameter mismatches on the controlled system. Though the internal resistance value of the inductor appears in the controller, we are not considering it's mismatch because it has minor influence on the control decision. Figure 5.8 shows the experimental results of the rectifier for an increase by $+30\%$ in the source inductance value L_s. Figure 5.9 shows the experimental results obtained for an increase by $+30\%$ in both capacitance values. For both tests the increase is done for the value of the parameter used in the controller and for equal load resistance values of 50 Ω. From both figures we observe that the controller is able to control the converter in order to deliver the required power to the loads though these parameters appear in the cost function which decides the next sampling time's control input. This shows the good robustness of the proposed FCS-MPC controller.

5.5 Conclusions

In this chapter, the design of a Lyapunov-based MPC applied to the 3-cell 7-level PUC rectifier is presented. The cost function of the proposed MPC is designed based on Lyapunov control method, where the converter is controlled from a stability point-of-view, with no gains associated with the cost function. The proposed controller uses the controlled system's model to predict the load currents; thus no current sensors are used for the loads. The advantages of the presented controller simplify the control algorithm and introduce the PUC converter as a good candidate for industrial applications.

Chapter 6

CONCLUSIONS AND FUTURE WORK

6.1 Coclusions

The new control methods and findings in this thesis helped in clearly understanding the operation principle of the PUC converter. The presented methods overcome the existing difficulties of the PUC and offer solutions which can be used in industrial applications. An operative well-organized and alternative control methods are introduced for the PUC multilevel converter which can be easily extended to other multilevel converter topologies, as well. These methods are characterized by their simplicity in design and implementation.

The Lyapunov-based model predictive control has the great feature of eliminating the gain associated with the cost function. This is true for two and three controlled variables as shown for the problem of grid connected inverter and dual output rectifier, respectively. In both problems the controller has shown more effective performance compared to conventional model predictive control. In addition, the Lyapunov-based MPC when applied to the PUC rectifier with dual output, the controller includes estimation of the load currents, where load current sensors are eliminated which is preferable in industrial applications. The controllers demonstrate excellent performance in terms of harmonic distortion, immunity to parameter mismatch, and robustness against disturbances.

In order to further improve the power quality of the inverter, sliding mode controller is used to control the PUC inverter. As it is difficult to design the control strategy as a standard sliding mode problem, a separate sliding line is designed for each controlled variable. This simplifies the controller design procedure with alleviates the need for gain tuning. The SM controller has low computational complexity, and introduces a direct relation between an allowable error in the auxiliary capacitor voltage and the hysteresis bandwidth parameter. Indeed introduction of the design parameter h leads to a reduction in the average switching frequency of the controller. Simulation and experimental results have proven the effectiveness of the SM controller in terms of dynamic performance, harmonic distortion, and robustness against disturbances and parameter mismatches.

6.2 Future Works

In the future work, the authors are targeting to work on the stability analysis of the PUC7 inverter when Lyapunov-based model predictive controller is used. The stability study aims to mathematically express the stable and unstable regions in a specific range, in accordance with system's variables and parameters. In chapter 3 it is shown that the region of the stability exists by simulating a .GIF figures where the stability region changes with time. A more rigorous approach will be used (if possible) to prove the stability region in a mathematical form.

In sliding mode theory, the idea of splitting the switching surfaces is very interesting. The same concept may be applied to the dual output PUC7 rectifier (or PUC5 rectifier). Additionally, the sliding mode controller concept can be linked directly to the operation principle of hysteresis controller. It will be interesting to study how the SMC works compared to the operation principle of the hysteresis controller.

On the other hand, all the proposed methods can be applied to the modified PUC5 [90] and modified PUC7 converters [91], for application such as dynamic voltage restorers, power factor correctors and active power filters. The control concept can be extended to 9 level PUC converters for single phase and three phase applications as well.

REFERENCES

[1] M. Trabelsi, S. Bayhan, K. A. Ghazi, H. Abu-Rub, and L. Ben-Brahim, "Finite-control-set model predictive control for grid-connected packed-U-cells multilevel inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7286–7295, Nov 2016.

[2] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *Power electronics for renewable energy systems, transportation and industrial applications*. John Wiley & Sons, 2014.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135–151, Jan 2016.

[4] A. Chen, L. Hu, L. Chen, Y. Deng, and X. He, "A multilevel converter topology with fault-tolerant ability," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 405–415, March 2005.

[5] K. J. Pratheesh, G. Jagadanand, and R. Ramchand, "A generalized-switch-matrix-based space vector modulation technique using the nearest level modulation concept for neutral-point-clamped multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4542–4552, June 2018.

[6] J. Weidong, L. Wang, J. Wang, X. Zhang, and P. Wang, "A carrier-based virtual

space vector modulation with active neutral-point voltage control for a neutral-point-clamped three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8687–8696, Nov 2018.

[7] E. Burguete, J. López, and M. Zabaleta, "A new five-level active neutral-point-clamped converter with reduced overvoltages," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7175–7183, Nov 2016.

[8] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, May 1996.

[9] M. Ghanes, M. Trabelsi, H. Abu-Rub, and L. Ben-Brahim, "Robust adaptive observer-based model predictive control for multilevel flying capacitors inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7876–7886, Dec 2016.

[10] H. Watanabe, T. Sakuraba, K. Furukawa, K. Kusaka, and J. Itoh, "Development of dc to single-phase ac voltage source inverter with active power decoupling based on flying capacitor dc/dc converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4992–5004, June 2018.

[11] E. Babaei and S. Laali, "Optimum structures of proposed new cascaded multilevel inverter with reduced number of components," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6887–6895, Nov 2015.

[12] R. Sajadi, H. Iman-Eini, M. K. Bakhshizadeh, Y. Neyshabouri, and S. Farhangi, "Selective harmonic elimination technique with control of capacitive dc-link voltages in an asymmetric cascaded h-bridge inverter for statcom application," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8788–8796, Nov 2018.

[13] T. Zhao, X. Zhang, W. Mao, F. Wang, J. Xu, Y. Gu, and X. Wang, "An optimized third harmonic compensation strategy for single-phase cascaded h-bridge photovoltaic inverter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8635–8645, Nov 2018.

[14] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector pwm - a modulation for the comprehensive neutral-point balancing in the three-level npc inverter," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 11–15, March 2004.

[15] P. M. Robina, F. Umbria, F. Salas, and F. Gordillo, "Integrated control of five-level diode-clamped rectifiers," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[16] A. Kahwa, H. Obara, and Y. Fujimoto, "Design of 5-level reduced switches count h-bridge multilevel inverter," in *Advanced Motion Control (AMC), 2018 IEEE 15th International Workshop on*. IEEE, 2018, pp. 41–46.

[17] S. Vazquez, J. I. Leon, J. M. Carrasco, L. G. Franquelo, E. Galvan, J. A. Sanchez, and E. Dominguez, "Controller design for a single-phase two-cell

multilevel cascade h-bridge converter," in *2008 IEEE International Symposium on Industrial Electronics*, June 2008, pp. 2342–2347.

[18] L. M. Kunzler and L. A. C. Lopes, "Power balance technique for cascaded h-bridge multilevel cells in a hybrid power amplifier with wide output voltage range," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2018, pp. 800–805.

[19] D. Mukherjee and D. Kastha, "A reduced switch hybrid multilevel unidirectional rectifier," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[20] S. Zhang, U. K. Madawala, and D. J. Thrimawithana, "A predictive controller for modular multi-level converters," in *2018 5th International Conference on Electric Power and Energy Conversion Systems (EPECS)*, April 2018, pp. 1–6.

[21] B. S. Riar, T. Geyer, and U. K. Madawala, "Model predictive direct current control of modular multi-level converters," in *2013 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2013, pp. 582–587.

[22] S. Kim, Y. Jang, and R. Kim, "Modeling and hierarchical structure-based model predictive control of cascaded flying capacitor bridge multilevel converter for active front-end rectifier in solid state transformer," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[23] Y. Ounejjar and K. Al-Haddad, "A novel high energetic efficiency multilevel topology with reduced impact on supply network," in *2008 34th Annual*

Conference of IEEE Industrial Electronics, Nov 2008, pp. 489–494.

[24] K. Al-Haddad, Y. Ounejjar, and L.-A. Gregoire, "Multilevel electric power converter," Patent, May 3, 2016, US Patent 9,331,599.

[25] Y. Ounejjar and K. Al-Haddad, "A new high power efficiency cascaded U cells multilevel converter," in *2009 IEEE International Symposium on Industrial Electronics*, July 2009, pp. 483–488.

[26] Y. Ounejjar, K. Al-Haddad, and L. A. Gregoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1294–1306, April 2011.

[27] Y. Ounejjar and K. Al-Haddad, "A novel high energetic efficiency multilevel topology with reduced impact on supply network," in *2008 34th Annual Conference of IEEE Industrial Electronics*, Nov 2008, pp. 489–494.

[28] ——, "A novel high energetic efficiency multilevel topology with reduced impact on supply network," in *2008 34th Annual Conference of IEEE Industrial Electronics*, Nov 2008, pp. 489–494.

[29] Y. Ounejjar, K. Al-Haddad, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3808–3816, Oct 2012.

[30] M. Sleiman, H. F. Blanchette, K. Al-Haddad, L. A. Gregoire, and H. Y. Kanaan, "A new 7L-PUC multi-cells modular multilevel converter for ac-ac and ac-dc applications," in *IEEE International Conference on Industrial Technology (ICIT)*, 2015.

[31] M. V. Onizuka, R. C. García, J. O. P. Pinto, and L. E. B. da Silva, "Current vector control based on average capacitor voltage strategy and hybrid modulation applied to the control of a 7-level puc three-phase inverter," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Dec 2016, pp. 1–6.

[32] S. Xiao, M. Metry, M. Trabelsi, R. S. Balog, and H. Abu-Rub, "A model predictive control technique for utility-scale grid connected battery systems using packed U cells multilevel inverter," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 5953–5958.

[33] M. Sleiman, H. F. Blanchette, L. A. Grégoire, H. Kanaan, and K. Al-Haddad, "Model predictive control of a dual output seven-level rectifier," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Nov 2015, pp. 005 292–005 297.

[34] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched dc sources," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3269–3278, July 2014.

[35] A. N. Babadi, O. Salari, M. J. Mojibian, and M. T. Bina, "Modified multilevel inverters with reduced structures based on packedu-cell," *IEEE Journal of*

Emerging and Selected Topics in Power Electronics, vol. 6, no. 2, pp. 874–887, June 2018.

[36] H. Vahedi, A. A. Shojaei, L. Dessaint, and K. Al-Haddad, "Reduced dc-link voltage active power filter using modified puc5 converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 943–947, Feb 2018.

[37] H. Vahedi, A. Dehghanzadeh, and K. Al-Haddad, "Static var compensator using packed u-cell based multilevel converter," in *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, April 2018, pp. 1–5.

[38] M. Trabelsi, H. Komurcugil, S. S. Refaat, and H. Abu-Rub, "Model predictive control of packed u cells based transformerless single-phase dynamic voltage restorer," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2018, pp. 1926–1931.

[39] ——, "Model predictive control of packed u cells based transformerless single-phase dynamic voltage restorer," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2018, pp. 1926–1931.

[40] J. D. Barros and J. F. Silva, "Optimal predictive control of three-phase npc multilevel converter for power quality applications," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 10, pp. 3670–3681, Oct 2008.

[41] F. Sebaaly, H. Vahedi, H. Y. Kanaan, and K. Al-Haddad, "Experimental design

of fixed switching frequency model predictive control for sensor-less five-level packed u-cell inverter," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[42] A. N. Babadi, O. Salari, M. J. Mojibian, and M. T. Bina, "Modified multilevel inverters with reduced structures based on packedu-cell," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 874–887, June 2018.

[43] S. Arazm, H. Vahedi, and K. Al-Haddad, "Phase-shift modulation technique for 5-level packed u-cell (puc5) inverter," in *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, April 2018, pp. 1–6.

[44] M. Trabelsi, H. Vahedi, H. Komurcugil, H. Abu-Rub, and K. Al-Haddad, "Low complexity model predictive control of puc5 based dynamic voltage restorer," in *2018 IEEE 27th International Symposium on Industrial Electronics (ISIE)*, June 2018, pp. 240–245.

[45] M. Trabelsi, S. Bayhan, M. Metry, H. Abu-Rub, L. Ben-Brahim, and R. Balog, "An effective model predictive control for grid connected packed u cells multilevel inverter," in *2016 IEEE Power and Energy Conference at Illinois (PECI)*, Feb 2016, pp. 1–6.

[46] H. Vahedi, P. A. Labbé, and K. Al-Haddad, "Sensor-less five-level packed U-cell (puc5) inverter operating in stand-alone and grid-connected modes," *IEEE*

Transactions on Industrial Informatics, vol. 12, no. 1, pp. 361–370, Feb 2016.

[47] S. Xiao, M. Metry, M. Trabelsi, R. S. Balog, and H. Abu-Rub, "A model predictive control technique for utility-scale grid connected battery systems using packed u cells multilevel inverter," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 5953–5958.

[48] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, Mar 2001.

[49] P. Cortés, M. P. Kazmierkowski, R. Kennel, D. E. Quevedo, and J. R. Rodriguez, "Predictive control in power electronics and drives." *IEEE Trans. Industrial Electronics*, vol. 55, no. 12, pp. 4312–4324, 2008.

[50] D. Q. Mayne, J. B. Rawlings, C. V. Rao, and P. O. Scokaert, "Constrained model predictive control: Stability and optimality," *Automatica*, vol. 36, no. 6, pp. 789–814, 2000.

[51] K. R. Muske and J. B. Rawlings, "Model predictive control with linear models," *AIChE Journal*, vol. 39, no. 2, pp. 262–287, 1993.

[52] D. E. Quevedo, R. P. Aguilera, and T. Geyer, "Predictive control in power electronics and drives: Basic concepts, theory, and methods," in *Advanced and Intelligent Control in Power Electronics and Drives*. Springer, 2014, pp. 181–226.

[53] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control a simple and powerful method to control power converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826–1838, June 2009.

[54] J. I. Metri, H. Vahedi, H. Y. Kanaan, and K. Al-Haddad, "Real-time implementation of model-predictive control on seven-level packed U-cell inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4180–4186, July 2016.

[55] F. Sebaaly, H. Vahedi, H. Y. Kanaan, and K. Al-Haddad, "Experimental design of fixed switching frequency model predictive control for sensor-less five-level packed u-cell inverter," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[56] H. Makhamreh, M. Sleiman, O. Kukrer, and K. Al-Haddad, "Lyapunov-based model predictive control of a puc7 grid-connected multilevel inverter," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2018.

[57] R. P. Aguilera, R. Baidya, P. Acuna, S. Vazquez, T. Mouton, and V. G. Agelidis, "Model predictive control of cascaded h-bridge inverters based on a fast-optimization algorithm," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Nov 2015, pp. 004 003–004 008.

[58] C. Qi, X. Chen, P. Tu, and P. Wang, "Cell-by-cell-based finite-control-set model predictive control for a single-phase cascaded h-bridge rectifier," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1654–1665, Feb 2018.

[59] T. Geyer and D. E. Quevedo, "Multistep finite control set model predictive control for power electronics," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6836–6846, Dec 2014.

[60] M. Norambuena, C. Garcia, J. Rodriguez, and P. Lezana, "Finite control set model predictive control reduced computational cost applied to a flying capacitor converter," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2017, pp. 4903–4907.

[61] M. Mosa, R. S. Balog, H. Abu-Rub, and M. Elbuluk, "A modified symmetric and asymmetric multilevel power inverter with reduced number of power switches controlled by mpc," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 488–493.

[62] W. Gao and J. C. Hung, "Variable structure control of nonlinear systems: A new approach," *IEEE transactions on Industrial Electronics*, vol. 40, no. 1, pp. 45–55, 1993.

[63] H. Makhamreh and O. Kukrer, "Discrete sliding mode control of lcl grid connected inverter under distorted grid voltage," in *2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018)*, April 2018, pp. 1–5.

[64] Q. Yang, M. Saeedifard, and M. A. Perez, "Sliding mode control of the modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 2, pp. 887–897, Feb 2019.

[65] O. Kukrer, H. Komurcugil, and A. Doganalp, "A three-level hysteresis function approach to the sliding-mode control of single-phase ups inverters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 9, pp. 3477–3486, Sept 2009.

[66] G. S. da Silva, R. P. Vieira, and C. Rech, "Discrete-time sliding-mode observer for capacitor voltage control in modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 876–886, Jan 2018.

[67] H. Makhamreh and O. Kukrer, "Discrete time sliding mode control of single phase lcl grid-inverter," in *2017 IEEE International Conference on Industrial Technology (ICIT)*, March 2017, pp. 84–88.

[68] N. Kumar, T. K. Saha, and J. Dey, "Sliding-mode control of pwm dual inverter-based grid-connected pv system: Modeling and performance analysis," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 435–444, June 2016.

[69] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[70] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, June 2008.

[71] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo,

B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[72] Z. Zhang, H. Fang, F. Gao, J. Rodríguez, and R. Kennel, "Multiple-vector model predictive power control for grid-tied wind turbine system with enhanced steady-state control performance," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6287–6298, Aug 2017.

[73] Z. Zhang, Z. Li, M. P. K. GAE, J. Rodriguez, and R. K. GAE, "Robust predictive control of three-level npc back-to-back converter pmsg wind turbine systems with revised predictions," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[74] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters —state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.

[75] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[76] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, June 1992, pp. 397–403 vol.1.

[77] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1130–1138, Sept 1996.

[78] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 508–516, March 2007.

[79] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1839–1846, June 2009.

[80] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 140–147, Jan 2006.

[81] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 769–778, Feb 2012.

[82] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 543–550, March 2008.

[83] J. Liu, X. Zhu, and J. Zeng, "A seven-level inverter with self-balancing and low voltage stress," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2018.

[84] M. Saeedian, S. M. Hosseini, and J. Adabi, "Step-up switched-capacitor module for cascaded mli topologies," *IET Power Electronics*, vol. 11, no. 7, pp. 1286–1296, 2018.

[85] S. S. Lee, "A single-phase single-source 7-level inverter with triple voltage boosting gain," *IEEE Access*, vol. 6, pp. 30 005–30 011, 2018.

[86] M. Ye, L. Kang, Y. Xiao, P. Song, and S. Li, "Modified hybrid modulation strategy with power balance control for h-bridge hybrid cascaded seven-level inverter," *IET Power Electronics*, vol. 11, no. 6, pp. 1046–1054, 2018.

[87] H. Komurcugil and O. Kukrer, "Lyapunov-based control for three-phase pwm ac/dc voltage-source converters," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 801–813, Sep 1998.

[88] J.-J. E. Slotine, W. Li *et al.*, *Applied nonlinear control*. Prentice hall New Jersey, 1991, vol. 199, no. 1.

[89] R. Gupta, A. Ghosh, and A. Joshi, "Multiband hysteresis modulation and switching characterization for sliding-mode-controlled cascaded multilevel inverter." *IEEE Trans. Industrial Electronics*, vol. 57, no. 7, pp. 2344–2353, 2010.

[90] H. Vahedi, A. A. Shojaei, L. Dessaint, and K. Al-Haddad, "Reduced dc-link voltage active power filter using modified puc5 converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 943–947, Feb 2018.

[91] H. Vahedi, M. Sharifzadeh, and K. Al-Haddad, "Modified seven-level pack u-cell inverter for photovoltaic applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1508–1516, Sep. 2018.