A Transformerless Step-Up DC-DC Converter

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ABSTRACT

In distributed generation (DG) systems, interfacing photovoltaic (PV) energy based sources to the grid poses a number of problems. Nowadays, transformerless converters are preferred for higher efficiency, low size and cost. Such a converter has its own problems. The output voltage of PV arrays is relatively low, requiring a high step-up converter to obtain the DC voltage input of the inverter.

In this project, a new step up converter proposed in a recent work [1], is analyzed, designed, simulated with MATLAB Simulink and practically implemented. Besides, the performance and effectiveness of some standard and improved boost converter circuits are discussed and compared in terms of voltage gain, power loss and switch voltage stress requirement. In fact, those performances are examined with deriving formulas and equations of current, voltages, power loss and voltage gain.

A major aim of the project is to investigate the effectiveness of this converter regarding application in DG systems. The improved effectiveness due to the lower power loss invoked with such a converter, which at the same time possesses a high voltage step up gain and a lower switch voltage stress compared to the standard boost converter. Theses characteristics together are attractive feature for use with DG systems.

Keywords: Transformerless, Boost Converter, Voltage Gain, DG Systems

ÖZ

Dağıtılmış üretim sistemlerinde (DÜS), güneş pilleri temelli enerji sistemlerini elektrik şebekesine bağlamak sorunlari yaratmaktadır. Günümüzde, trafosuz çevirgeçler yüksek verimlilik, düşük hacim ve maliyet gerekçeleri ile tercih edilmektedir. Fakat, böyle bir çevirgeçin de kendine göre sorunları vardır. Güneş pil dizilerinin çıkış gerilimleri genellikle düşüktür veçevirgeçin giriş gerilimini elde etmek için yüksek kazançlı bir DC-DC çevirgeçe ihtiyaç vardır.

Bu projede, yakın zamanlarda önerilen yeni bir yükselticinin analizi, tasarımı, MATLAB Simulinkle simülasyonu ve deneysel uygulaması yapılmıştır. Bunun yanında, bazı standard ve iyileştirilmiş çevirgeç devrelerinin performans ve etkinlikleri tartışılıp, kazanç, güç kaybı ve anahtar üzerindeki gerilim baskısı bakımından karşılaştırmaları yapılmıştır. Bu çevirgeçlerin performansları, akım gerilim ve güç kaybı denklemleri elde edilerek değerlendirildi.

Bu projenin başlıca amacı bu tip yükselteçlerin DÜS uygulamaları bakımından etkinliğini araştırmaktır. Bu çevirgeçlerin standard yükselticilere göre iyileştirilmiş etkinliği daha yüksek gerilim kazancı ve daha düşük anahtar gerilimi baskısından kaynaklanmaktadır. Bunlar DÜS'lerde uygulama için çekici özelliklerdir.

Anahtar kelimeler: Trafosuz, Yükseltici Çevirgeç, Gerilim Kazancı, Dağıtılmış Üretim Sistemleri.

To my father and mother, brothers and sisters

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LIST OF ABBREVIATIONS/SYMBOLS

AC	Alternating Current
BJT	Bipolar Junction Transistor
C	Capacitor value
CCM	Continuous Conduction Mode
CFL	Compact Fluorescent Light
D	Duty cycle
DC	Direct Current
DCM	Discontinuous Conduction Mode
DG	Distributed Generation
E	Energy stored in the inductor
IGBT	Insulated Gate Bipolar Transistor
L	Inductor value
LCD	Liquid Crystal Display
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NPT	Non-Punch Through
P	Power Switching loss
PT	Punch Through
PV	Photo-Voltaic
S	Switch
SCRs	Silicon-Controlled Rectifiers
SMPS	Switching-Mode Power Supply
T	Total time period
t	Time period
C_0	Output Capacitor
C1	The First Capacitor value
C2	The Second Capacitor value

D_0	Output Diode
D_1	Diode number One
D_2	Diode number Two
ΔI_L	the variation Inductor current
ΔI_{LOff}	the variation Inductor current during off-state
ΔI_{LOn}	the variation Inductor current during on-state
f_s	Switching Frequency
I_{Co}	Output Capacitor Current
I_D	Diode Current
I_L	Inductor Current
I_{L1p}	Parallel Currant during Inductor number One
I_{L2p}	Parallel Currant during Inductor number Two
ΔI_{LOff}	the variation Inductor current during off-state
ΔI_{LOn}	the variation Inductor current during on-state
I_{LMax}	Maximum inductor current
I_S	Switch Current
L_1	Inductor number One
L_2	Inductor number Two
L_1	Inductor number One
R	The value of Output Resistant
S_1	Switch number One
S_2	Switch number two
δ	Constant
t_0	Time at the start point
t_1	Time at the point One
τ_{LB}	The Inductor Time constant for Boundary Condition
T_s	Switch constant time
V_{D3}	The third Diode Voltage
V_i	Input Voltage
V_{L1}	The First Inductor Voltage

V_{L2}	The Second Inductor Voltage
V_S	Switch Voltage
V_{s1}	Voltage Switch number One
V_{s2}	Voltage Switch number Two

Chapter 1

INTRODUCTION

Power electronics, as defined by Thomas G. Wilson, is:" The technology associated with the efficient conversion, control and conditioning of electric power by static means from its available input form into the desired electrical output form." The goal of power electronics is to realize power conversion from an electrical source to an electrical load in a highly efficient, highly reliable and cost-effective way.

The application of power electronics includes a variety of fields such as energy storage, transmission and distribution, pollution avoidance, communication, computer systems, propulsion and transportation .Power electronics modules are key units in power electronics system. As the integration of power switches, device gating, sensors, controls and actuators, power modules can be used to perform energy transfer, storage and conditioning.

According to the type of the input and output power, power conversion systems can be classified into four main categories, namely:

- AC to DC (rectification)
- DC to AC (inversion)
- AC to AC(cycloconversion)
- DC to DC(chopping)

A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC output voltage which is-typically- at a different voltage level than the input.

Apart from voltage level conversion, DC-to-DC converters are used to provide noise isolation, power bus regulation.

The typical usage of DC-DC converters is to convert unregulated dc voltage to regulated or variable dc voltage at the output. The output voltage in DC-DC converters is generally controlled using a switching concept. In fact, early DC-DC converters were known as choppers with silicon-controlled rectifiers (SCRs) used as the switching mechanism. Nowadays, Modern DC-DC converters employ insulated gate bipolar transistors (IGBTs) and metal oxide silicon field effect transistors (MOSFETs) as they possess attractive switching capabilities, especially in terms of switching frequency and power ratings.

Based on their performances, DC-DC converters are subcategorized into three general types; Buck Converters which convert from a voltage level to a relatively lower voltage level. Conversely, Boost Converters transform to higher voltage level. The third one is buck-boost converter which can either be a buck or a boost converter based on its control signals.

1.1 The High Step-Up (Boost Converter)

A boost (step-up) converter is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

This kind of converter has the advantages of simplicity and high efficiency. Besides, it is transformerless and thus has the desirable features of high efficiency, low cost and small size. However, it has high output ripple and it can not control short circuit current.

1.2 The Boost Converter Applications

High step up (Boost) converter is used in many applications such as discharge lamp for automobile, fuel cell energy conversion systems, and solar cells. The boost converter can also produce higher voltage to operate cold cathode florescent tube (CFL) in devices such as LCD back light and some flash lights. Moreover, DC-DC converters are building blocks of distributed power supply systems in which a common DC bus voltage is converted to various other voltages according to requirements of particular loads. Such distributed DC systems are common in space stations, ships and airplanes, as well as in computer and telecommunication equipment. It is expected that modern portable wireless communication and signal processing systems will use variable supply voltages to minimize power consumption and to extend battery life. Besides, the boost converter is also used to

solve problems invoked with interfacing the output voltage of photo-voltaic (PV) cells to grid, as will be explained in detail throughout this thesis.

1.3 Problem Statement

Photovoltaics (PV) is a method of generating electrical power by converting solar radiation into direct current electricity using semiconductors that exhibit the photovoltaic effect. In distributed generation (DG) systems, interfacing photovoltaic (PV) energy-based sources to the grid poses a number of problems. Nowadays, transformerless converters are preferred for higher efficiency and low size and cost. Such a converter has its own problems. The output voltage of PV arrays is relatively low, requiring a high step-up converter to obtain the dc voltage input of the inverter as depicted in Figure 1.1.

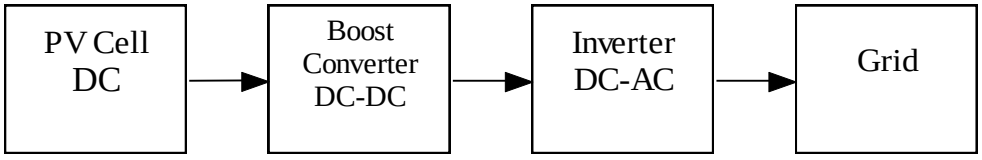


Figure 1.1: PV Power Generation Block Diagram

The objective of this project is to analyze, design and simulate a new step-up converter proposed in [1]. Research also includes investigation of the effectiveness of this converter application in DG systems.

1.4 Thesis Outline

This report is organized in four chapters; Chapter 1 offers a preface about power electronic converters focusing of Boost converters. Besides, the problem statement is addressed.

Chapter 2 reviews DC-DC converters in general, investigating the theory of transformerless DC-DC converters with high step-up voltage gain.

Chapter 3 is dedicated to discuss three main transformerless converter topologies that provide high voltage gain. This chapter presents the theory suggesting the raise in voltage gain verified by simulation under the MATLAB Simulink environment.

Chapter 4 is delivered the practical implantation result of two boost converter circuits the simple boost converter and the basic boost converter

Finally, Chapter 5 sums up the conclusions developed through this project, and addresses possible future works and extensions to the research conducted herein.

Chapter 2

BOOST CONVERTER

2.1 Introduction

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

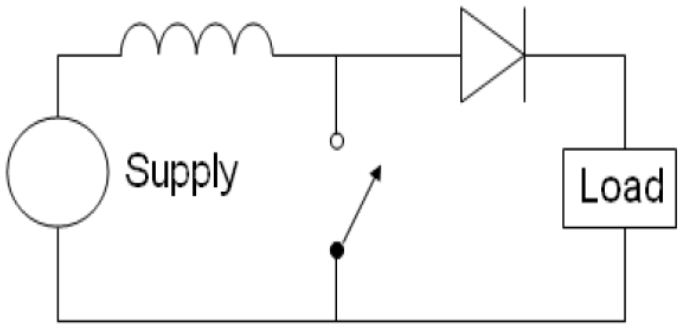


Figure 2.2: Basic Schematic of a Boost Converter. The switch is typically a MOSFET, IGBT or BJT

The operation of a boost converter is to boost or step-up a certain input voltage to a higher level, at the same time the boost converter steps-down the current as a natural result of the energy conservation principle, which implies that power, being the product of voltage and current, must be conserved.

The following section addresses the principle of operation of boost converter.

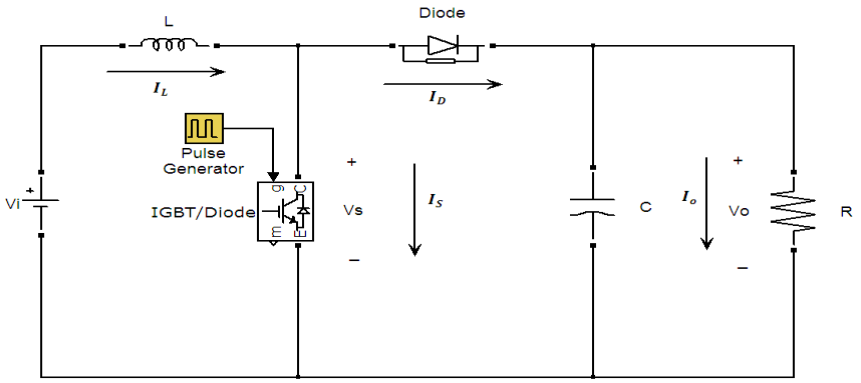
2.2Boost Converter Modes of Operation

The operation of the boost converter is essentially based on the tendency of an inductor to resist changes in its current. When an inductor is charged, it behaves like a load as it absorbs energy. On the other hand, when it is discharged, it behaves as an energy source.

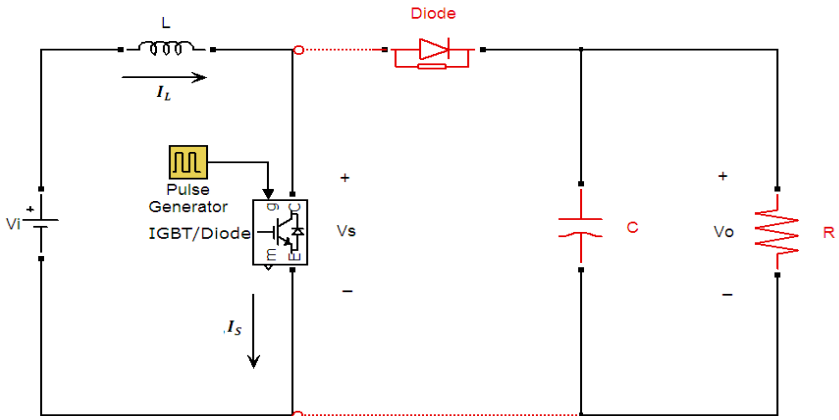
The fundamental idea behind the boost effect is the fact that the inductor's voltage during a discharging process depends only on the rate of change of its current with respect to time, and this voltage is independent of the source voltage by which the inductor was charged. This independency gives the possibility of having an output voltage greater than the input voltage.

The operation of boost converter is explained in Figure 2.2. It includes two distinct stages:

- The On-state: in which the switch is closed, and thus the inductor is charged, i.e., its current increases.(Figure 2.2-b)
- The Off-state: the switch is open and the only path offered to inductor current is through the diode D, the capacitor C and the load R. This results in transferring the energy accumulated during the On-state into the capacitor.(Figure 2.2-c)



(a)



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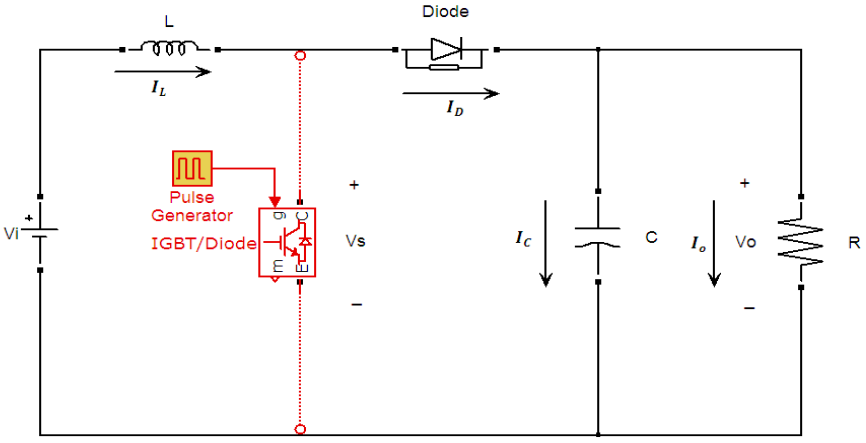

(c)

Figure 2.2: The Boost Converter with IGBT Switch Cases:

(a): General Schematic
(b): In the On-State
(c): In the Off-State

The boost converter has two modes of operation; the continuous mode (CCM) and the discontinuous mode (DCM), as will be explained in the following two subsections.

2.2.1 The Continuous Mode of Operation

As the name suggests, the inductor current in this mode does not fall to zero, this mode is illustrated in Figure 2.3 which shows the typical waveforms of currents and voltages.

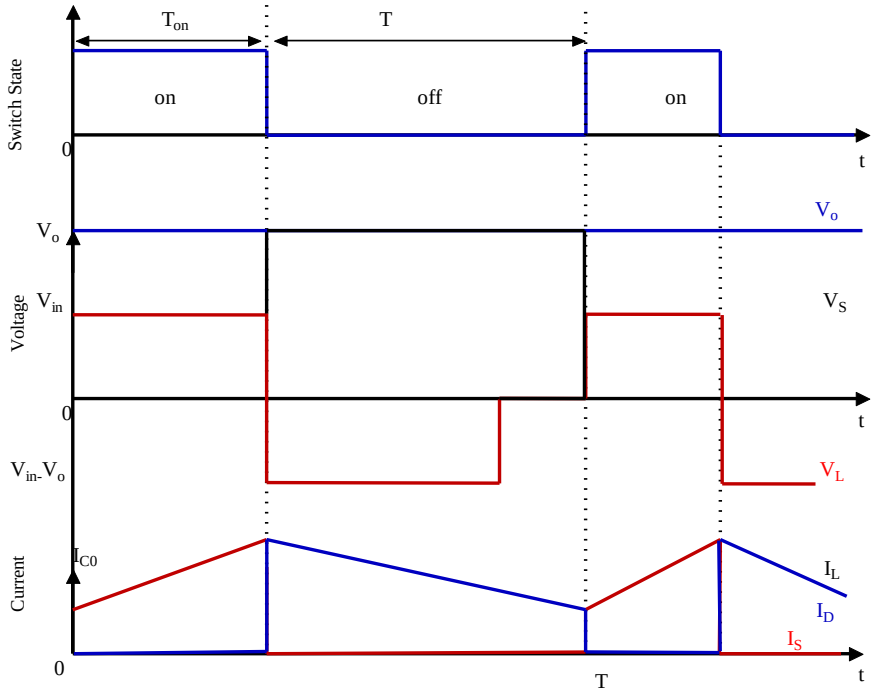

Figure 2.3: Current and Voltage Waveforms in a Boost Converter in the CCM

In a converter operating in this mode, the output voltage can be calculated as follows; in the case of an ideal converter (i.e using components with an ideal behaviour) operating in steady conditions:

During the On-state, the switch S is closed, which makes the input voltage (V_i) appear across the inductor, which causes a change in current (I_L) flowing through the inductor during a time period t to be as in (2.1):

$$\frac{\Delta I_L}{t} = \frac{V_i}{L} \tag{2.1}$$

At the end of the On-state, the increase of i_L is therefore:

$$\Delta I_{LOn} = \frac{1}{L}\int_0^{DT} V_i\, dt = \frac{DT}{L}V_i \qquad (2.2)$$

D is the duty cycle. It represents the fraction of the commutation period T during which the switch is on. Therefore D ranges between 0 (S is never on) and 1 (S is always on).

During the Off-state, the switch S is open, so the inductor current flows through the load. If we consider zero voltage drop in the diode, and a capacitor large enough for its voltage to remain constant, the evolution of I_L is:

$$V_i - V_0 = L\frac{di_L}{dt} \qquad (2.3)$$

Therefore, the variation of I_L during the Off-period is:

$$\Delta I_{LOff} = \int_0^{(1-D)T} T\,\frac{(V_i - V_o)dt}{L} = \frac{(V_i - V_o)(1-D)T}{L} \qquad (2.4)$$

As we consider that the converter operates in steady-state conditions, the amount of energy stored in each of its components has to be the same at the beginning and at the end of a commutation cycle. In particular, the energy stored in the inductor is given by 2.5.

$$E = \frac{1}{2}L{I_L}^2 \qquad (2.5)$$

Therefore, the inductor current has to be the same at the beginning and the end of the commutation cycle. This can be written as

$$\Delta I_{On} + \Delta I_{Off} = 0 \qquad (2.6)$$

Substituting ΔI_{LOn} and ΔI_{LOff} by their expressions yields:

$$\Delta I_{LOn} + \Delta I_{LOff} = \frac{V_i DT}{L} + \frac{(V_i - V_o)(1-D)T}{L} = 0 \qquad (2.6)$$

This can be written as:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{2.7}$$

This in turns reveals the duty cycle to be:

$$D = 1 - \frac{V_i}{V_o} \tag{2.8}$$

From the above expression it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D, theoretically to infinity as D approaches 1. This is why this converter is sometimes referred to as a *step-up* converter.

2.2.2The Discontinuous Mode of Operation

In some cases, the amount of energy required by the load is small enough to be transferred in a time smaller than the whole commutation period. In this case, the current through the inductor falls to zero during part of the period. The only difference in the principle described above is that the inductor is completely discharged at the end of the commutation cycle (see waveforms in figure 2.4).

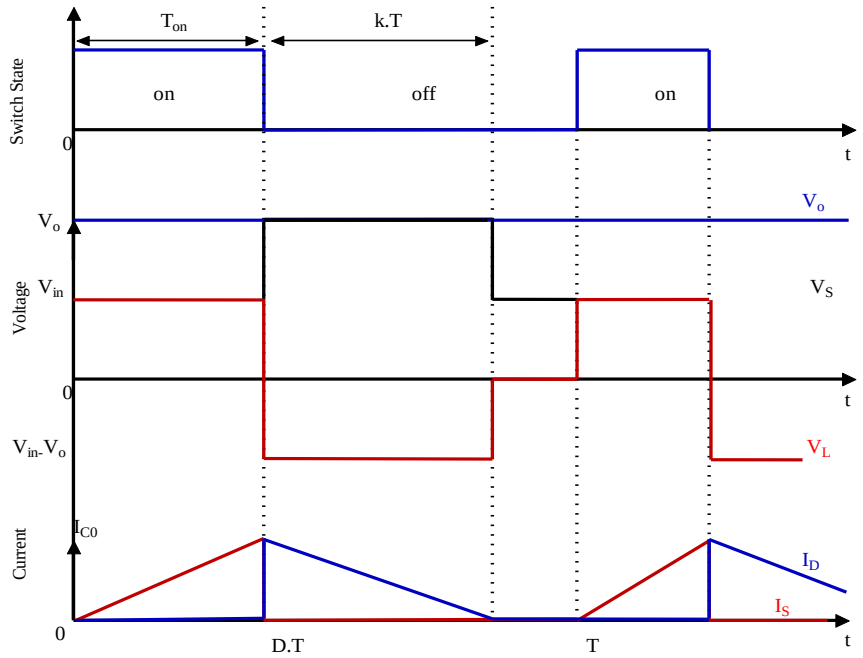

Figure 2.4: Current and Voltage Waveforms in a Boost Converter in the DCM

Although slight, the difference has a strong effect on the output voltage equation. It can be calculated as follows:

As the inductor current at the beginning of the cycle is zero, its maximum value I_{LMax} (at $t = DT$) is

$$I_{LMax} = \frac{V_i DT}{L} \tag{2.9}$$

During the off- period, I_L falls to zero after δT:

$$I_{LMax} + \frac{(V_i - V_o)kT}{L} = 0 \tag{2.10}$$

Using the two previous equations δ is:

$$k = \frac{V_i D}{V_o - V_i} \tag{2.11}$$

The load current I_o is equal to the average diode current (I_D). As can be seen on figure 4, the diode current is equal to the inductor current during the off-state. Therefore the output current can be written as:

$$I_O = I_D = \frac{I_{max}}{2} k \tag{2.12}$$

Replacing I_{max} and δ by their respective expressions yield:

$$I_o = \left(\frac{V_i DT}{2L}\right)\left(\frac{V_i D}{V_o - V_i}\right) = \frac{V_i^2 D^2 T}{2L(V_o - V_{in})} \tag{2.13}$$

Therefore, the output voltage gain can be written as follows:

$$\frac{V_o}{V_i} = 1 + \frac{V_i D^2 T}{2LI_o} \tag{2.14}$$

Compared to the expression of the output voltage for the continuous mode, this expression is much more complicated. Furthermore, in discontinuous operation, the output voltage gain not only depends on the duty cycle, but also on the inductor value, the input voltage, the switching frequency, and the output current.

2.3 IGBT

Insulated Gate Bipolar Transistor (IGBT) is one of the most popular applications in power switches. The special characteristic of the switch are in between the characteristic of Bipolar Junction Transistor (BJT) and MOS Field Effect Transistor (MOSFET). The only different between the structure of MOSFET and IGBT is the additional of P-zone of IGBT. Due to the present of this layer, holes are injected into the highly resistive n-layer and a carrier overflow is created. These increase the conductivity of n-layer and reduce the on-state voltage of IGBT. Figure 2.5 demonstrates the layer stricter of an IGBT.

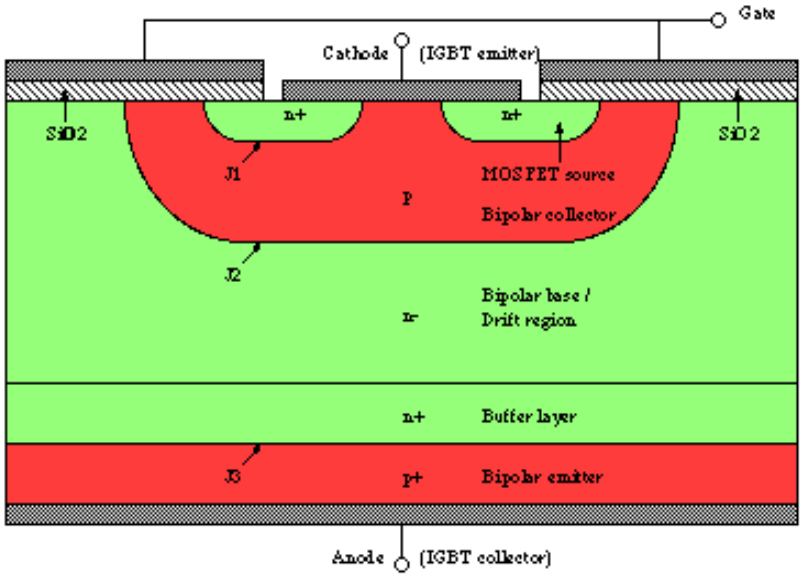

Figure 2.5: Demonstration of the IGBT Layer Structure [2]

To suit today application there are two types of IGBT, PT-structure (punch through) and NPT-structure (non-punch through). The general switching behaviour of IGBT, when the switch is turn–off the current are driven on by the load, by attaching suitable diode to enable the current flow. Then switching on the IGBT, the current flown the diode causes the circuit work like a short at first. The stored charged has to

be removed first for the diode to block the voltage. This appears as a surplus current additional to the load current which is called reverse recovery current of the diode.

The maximum reverse recovery current of diode occur when the sum of the instantaneous voltage across the IGBT and the diode equal to the supply voltage. By turning-off the IGBT result in current change and makes an over voltage spike by the current change in the parasitic inductances. Short circuit behaviour of IGBT generally define the negative temperature coefficient of the short circuit current causes the negative thermal feedback in the devices. There is two type of short circuit, the first type short-circuit describes the turn-on of an IGBT during the existing short-circuit in the output circuit. In this case the IGBT limits the maximum collector current according to the outputs characteristic. In the second type of short-circuit in the output circuit occur during the on-phase of the IGBT, limited by the inductivity the current in the output circuit increases.

2.4 Switching Losses

If an ideal switch were used in a boost converter, current would pass through the switch in the instant it is switched on, and it would fall to zero exactly in the instant the switch is switched off. However, this is not the case exhibited in practice as shown in Figure 2.6, where switches are not ideal so that there is a certain time period before charges are released off the switch, and another time period for the switch to establish a current path. The result of having this time latency is a switching power loss which equals the product of the current and voltage of the switch during the switch on and switch off times. [3]

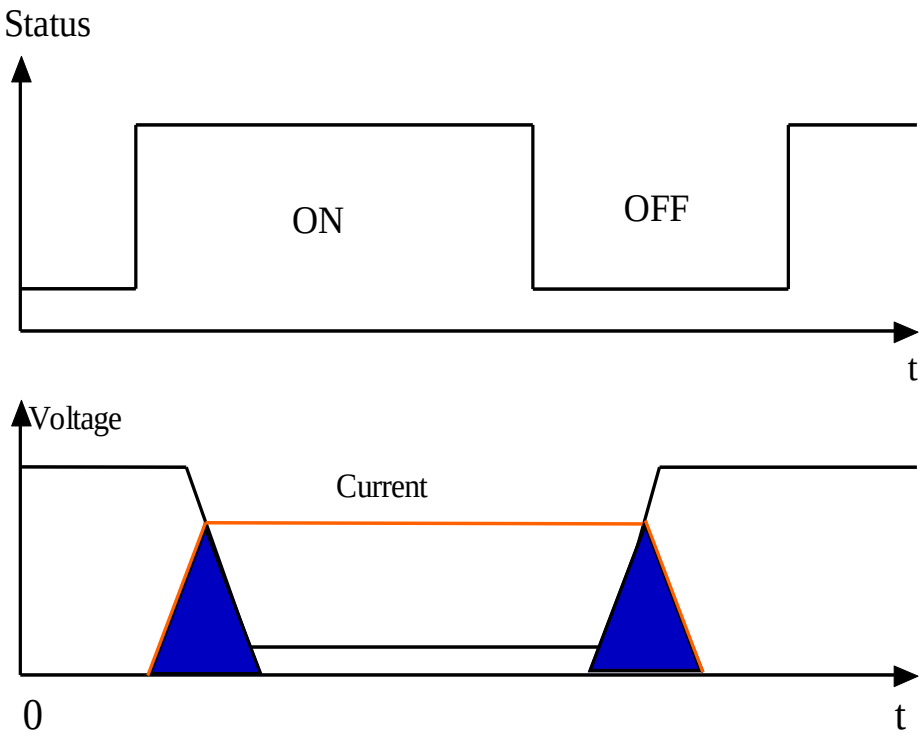

Figure 2.6 Boost Converter Switching Losses (Shaded area represents power loss)

Apart from switching losses, a boost converter also includes some other losses, namely, inductor resistance, the transistor on-stage voltage drop, and the forward voltage drop across the diode. According to [4], the effect of losses on the dc gain-duty ratio relationship is as shown in Figure.

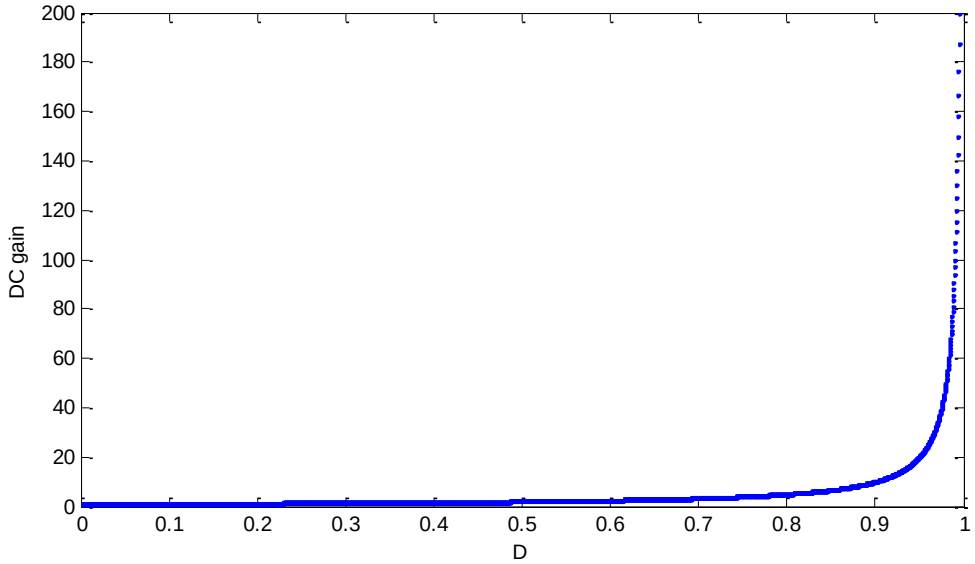

Figure 2.7: Effect of duty ratio on dc gain in boost converter

As shown in Figure 2.7, the gap between the actual and ideal dc gains increases with increasing the duty cycle. This increase in the gap is because the switch utilization is poor at high duty cycles so that their losses are higher. Moreover, switching losses also impose an upper limit on the switching frequency of a boost converter.

During the switching transitions, the transistor voltage and current are simultaneously large. In consequence, the transistor experiences high instantaneous power loss. This can lead to significant average power loss, even though the switching transitions are short in duration. Switching loss causes the converter efficiency to decrease as the switching frequency is increased. Also the DC gain goes to infinity when the duty cycle reaches one as pointed out by (2.15).

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{2.15}$$

Moreover, several mechanisms lead to switching loss. Significant energy can be lost during the slow switching times of minority-carrier semiconductor devices such as BJTs, IGBTs, and thyristors. The diode reverse recovery process induces substantial additional energy loss in the transistor during the transistor turn-on transition. The energy stored in the semiconductor output capacitances is dissipated during the transistor turn-on transition. Energy stored in transformer leakage inductances and other stray inductances is usually dissipated by the transistor during the turn-off transition. The total switching loss is equal to the sum of the energy losses that arise via these mechanisms, multiplied by the switching frequency.

Chapter 3

TRANSFORMERLESS BOOST CONVERTER WITH IMPROVED VOLTAGE GAIN

3.1 Introduction

This chapter discusses some boost converter topologies with improved voltage gain. Figure 3.1 shows the basic boost converter circuit from which the other topologies are obtained. As shown in the figure, this topology uses inductor technique, in which two inductors with the same level of inductance are charged in parallel during the switch-on period, and are discharged in series during the switch-off period to achieve high step up voltage gain without the extremely high duty ratio. Besides, this topology has four diodes that guarantee the required power current flow during the on and off states.

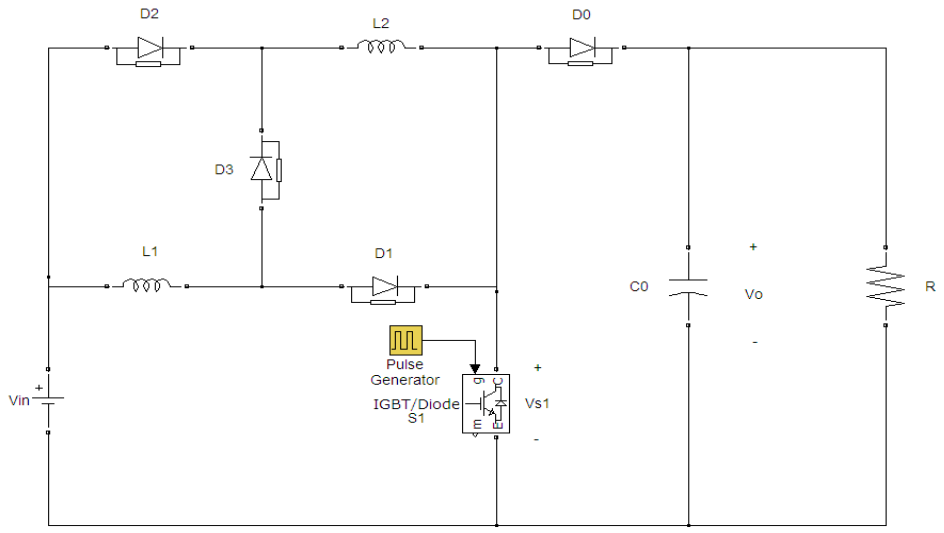

Figure 3.1: The Basic Converter Topology

Considering the circuit of Figure 3.1, the converter has two issues; during the switch-on period the current passes through three power devices, but during the switch-off period two power devices exist in the current flow path. Besides, the voltage stress when the switch is on equals the output voltage. On the other hand, when the switch is in the off-period, the output voltage equals the sum of the source voltage and the two inductor voltages i.e., the inductor voltages boost or raise the output voltage.

Figure 3.2 shows typical current and voltage waveforms of the basic boost converter circuit depicted in Figure 3.1.

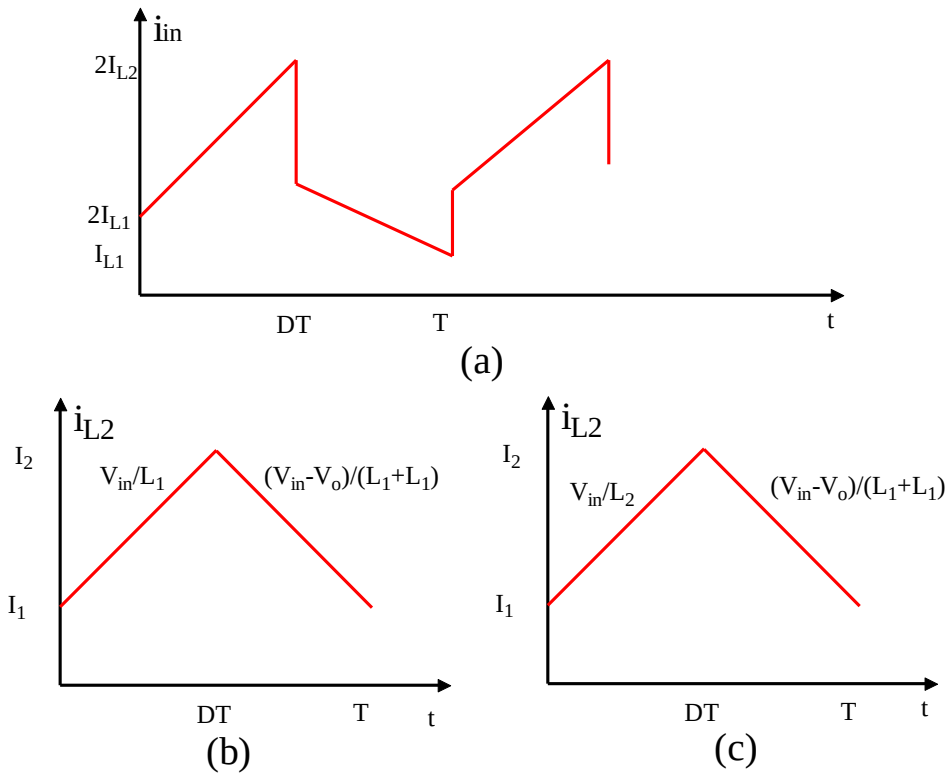

Figure 3.2: Typical Basic Converter Current and Voltage Waveforms

a: Input Current

b: First Inductor Current

c: Second Inductor Current

The operation of the circuit shown in Figure 3.1 and based on Figure3.2 can be divided into two distinct modes:

The continuous current mode: where the two inductors are in parallel, and thus:

$$I_2 = I_1 + \frac{V_{in}}{L_1} DT \tag{3.1}$$

, but the value of L_1 and L_2 are equal

$$L = L_1 = L_2 \tag{3.2}$$

, so the current I_2 becomes

$$I_2 = I_1 + \frac{V_{in}}{L} DT \tag{3.3}$$

During the interval [DT,T] the switch turns off and the current in the I_1 is given by

$$I_1 = I_2 + \frac{(V_{in} - V_o)}{2L}(1 - D) \tag{3.4}$$

, so by equating (3.4) and (3.5) and simplifying,

$$\frac{(V_{in} - V_o)}{2L}(1 - D)T = \frac{V_{in}}{L_2} D \tag{3.6}$$

$$(V_o - V_{in})(1 - D) = 2DV_{in} \tag{3.7}$$

From formula (3.7) the voltage gain is obtained as:

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{3.8}$$

During interval [0,DT] the input current is equal the to sum of I_{L1} and I_{L2}

$$i_{in} = i_{L1} + i_{L2} \tag{3.9}$$

, by plugging (3.1) into (3.2) and using (3.4) and (3.3) the input current becomes ,

$$i_{in} = 2I_1 + \frac{2V_{in}}{L} t \tag{3.10}$$

During time interval [DT,T] the input current $i_{in}$is equal to $I_{L1}$and also equal to I_{L2} the input current can be obtained as follows.

$$i_{in} = i_{L1} = i_{L2} \tag{3.11}$$

$$i_{in} = I_2 + \frac{(V_{in} - V_o)}{2L} t \tag{3.12}$$

To obtain the input current at duty cycle D by using conservative power law

$$P_{in} = P_O \tag{3.13}$$

, and

$$P_O = \frac{V_O^2}{R} \tag{3.14}$$

By plugging (3.12) into (3.13) and by using (3.14) the input current becomes as in (3.15).

$$I_{in} = \frac{(1+D)}{(1-D)^2} \frac{V_{in}}{R} \tag{3.15}$$

From Figure 3.2 the input current during time interval [0,T] is given by.

$$I_{in} = \frac{\{(\frac{2I_1 - 2I_2}{2})\mathrm{DT} + \left(\frac{I_1 - I_2}{2}\right)(1-D)T\}}{T} \tag{3.16}$$

By simplifying equation (3.16) the input current is obtained as

$$I_{in} = \left(\frac{I_1 + I_2}{2}\right)(1 + D) \tag{3.17}$$

By equating equation (3.15) and (3.17)

$$I_1 + I_2 = \frac{2}{(1-D)^2} \frac{V_{in}}{R} \tag{3.18}$$

By substitution of (3.17) in (3.18) the currents passing through L_1 is given by ,

$$I_1 = V_{in}[\frac{2}{R(1-D)^2} - \frac{D}{2Lf_s}] \tag{3.19}$$

In continuous current mode the current I_1 is greater than zero, so the frequency can be obtained as:

$$f_s > \frac{RD(1-D)^2}{2L} \tag{3.20}$$

From equation (3.8), the relationship between voltage gain and duty cycle is plotted in Figure 3.3.

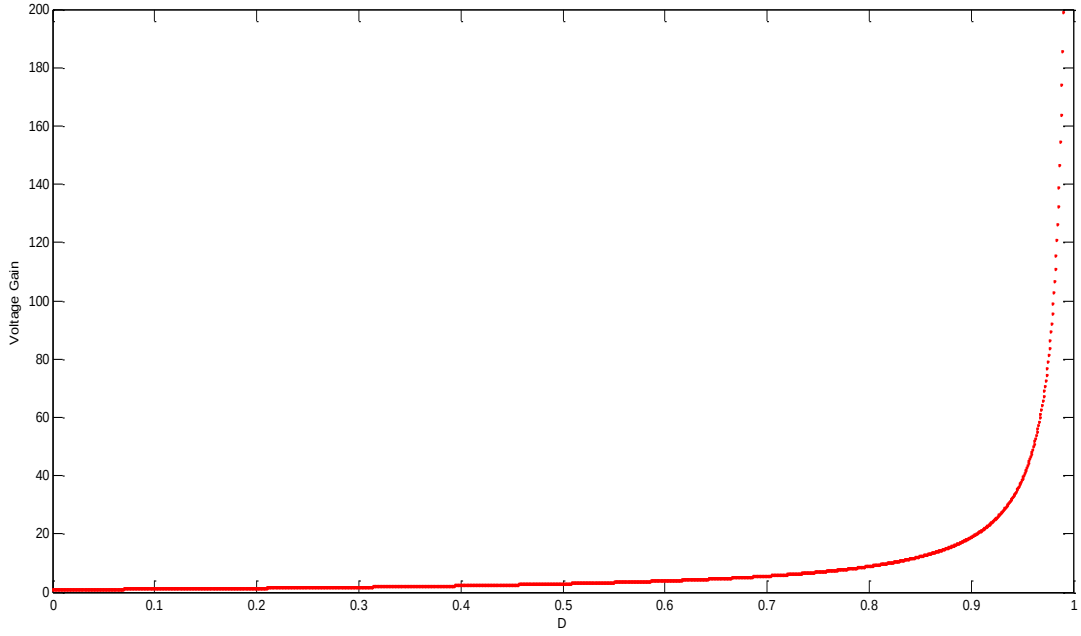

Figure 3.3: The Voltage Gain versus the Duty Cycle for Basic Converter Topology

3.2 Calculations and Simulation Results of the Basic Topology

This section presents simulation result of the basic topology in Fig .3.1 by using MATLAB Simulink .From reference [1] the value that are used L_1=$L_{2=}$100μH , P_o= 40W , $V_{IN} = 12V$, $V_o = 100V$ and C_o=68μF , f_s=100KHz and the pure resistive load is obtained according to the formula:

$$R_{O=}\frac{V_o^2}{P_o}=\frac{100^2}{40}=250\Omega \tag{3.21}$$

From (3.21), the duty cycle D is calculated as,

$$\frac{V_o}{V_{in}}=\frac{1+D}{1-D}=\frac{100}{12} \tag{3.22}$$

D=0.7857= 78.57%

Figure 3.4 shows the output voltage V_o and Figure 3.5 delivered V_{DO} and also Figure 3.6 and Figure 3.7 shows the current during inductors I_{L1}, I_{L2} and Figure 3.8the current passed in the output capacitor I_{Co} and Figure 3.9 shows the output current $I_o$finally Figure 3.10 delivers voltage switch stress V_{s1}.

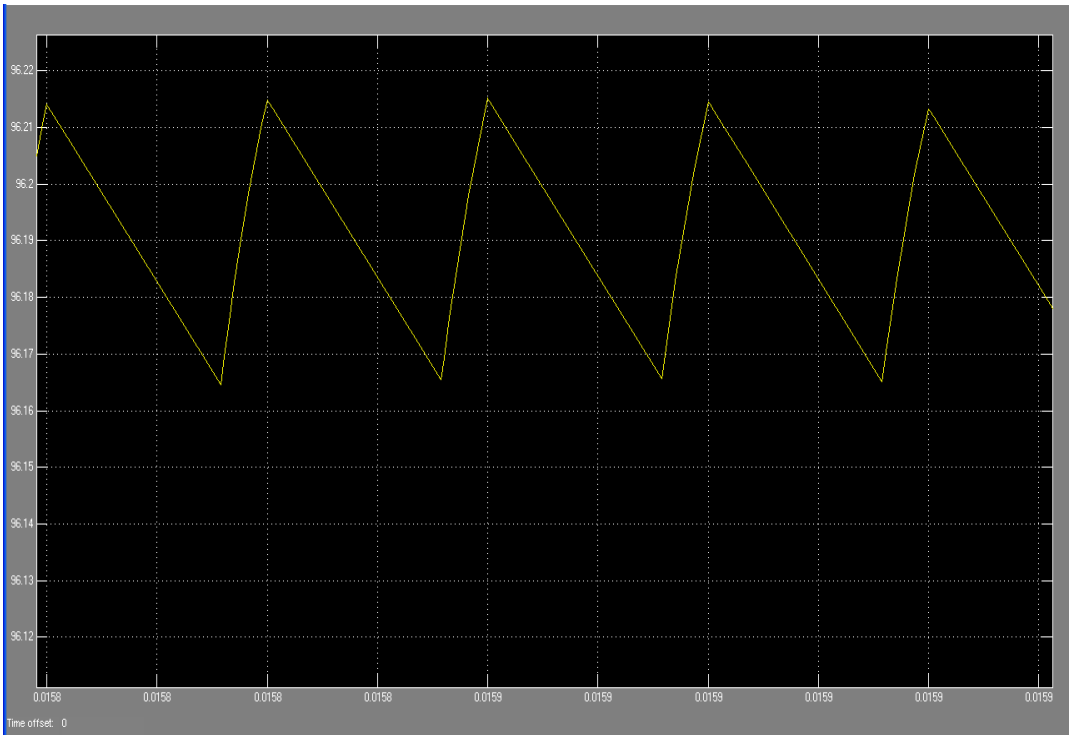

Figure 3.4The Output Voltage of Basic Converter Topology

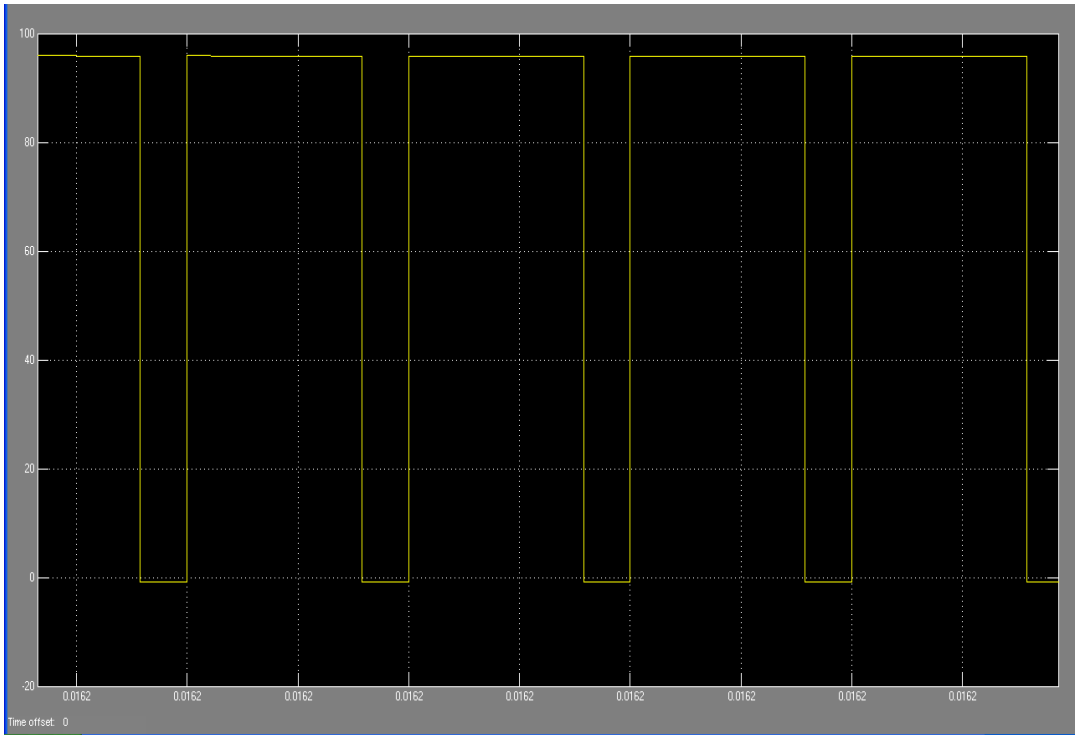

Figure 3.5: The Diode Voltage of Basic Converter Topology

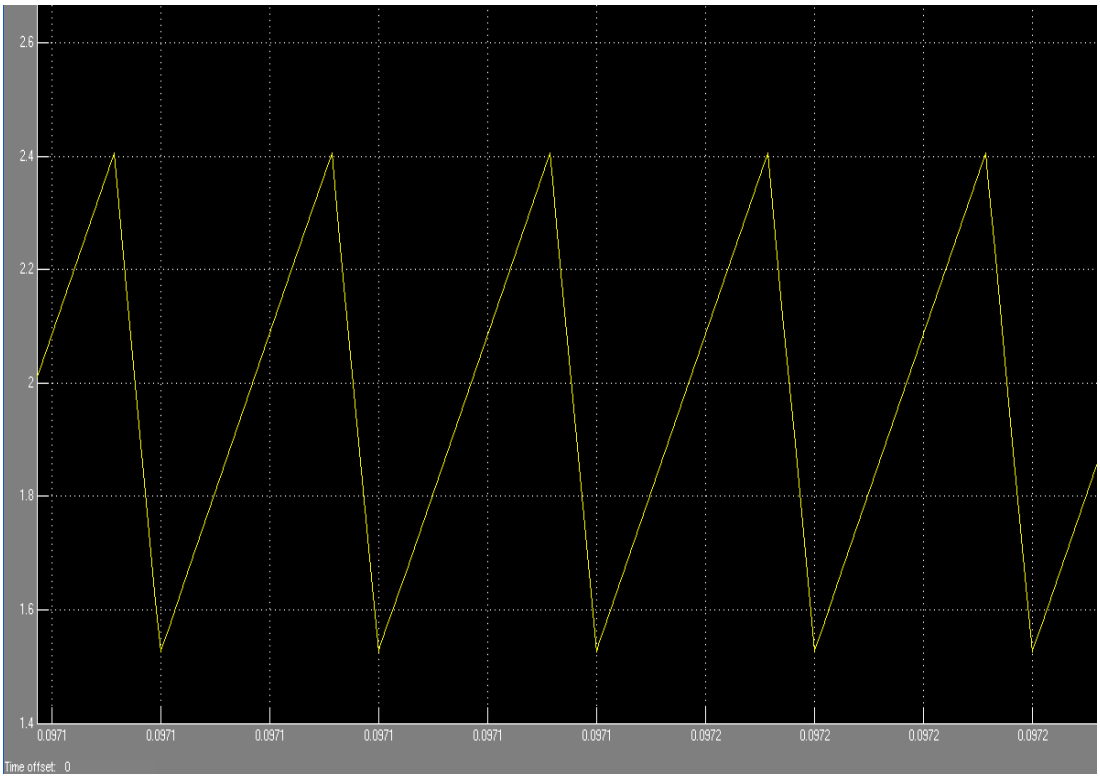

Figure 3.6: The L_1 Current of Basic Converter Topology

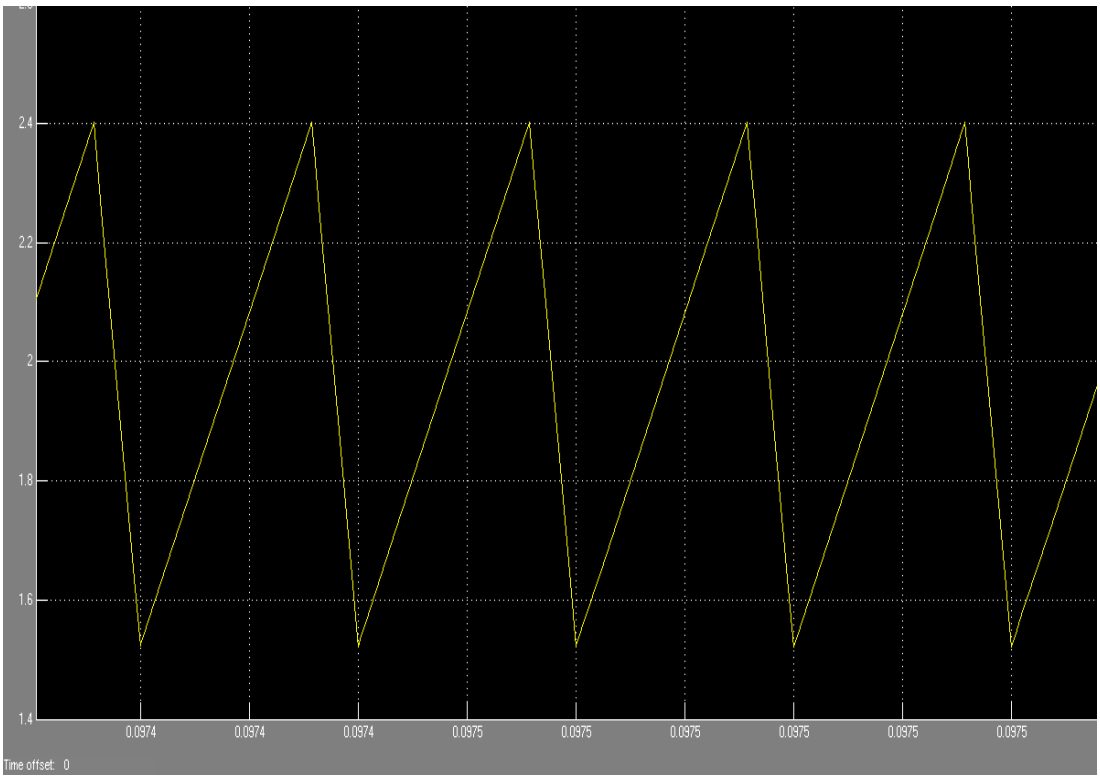

Figure 3.7: The L_2 Current of Basic Converter Topology

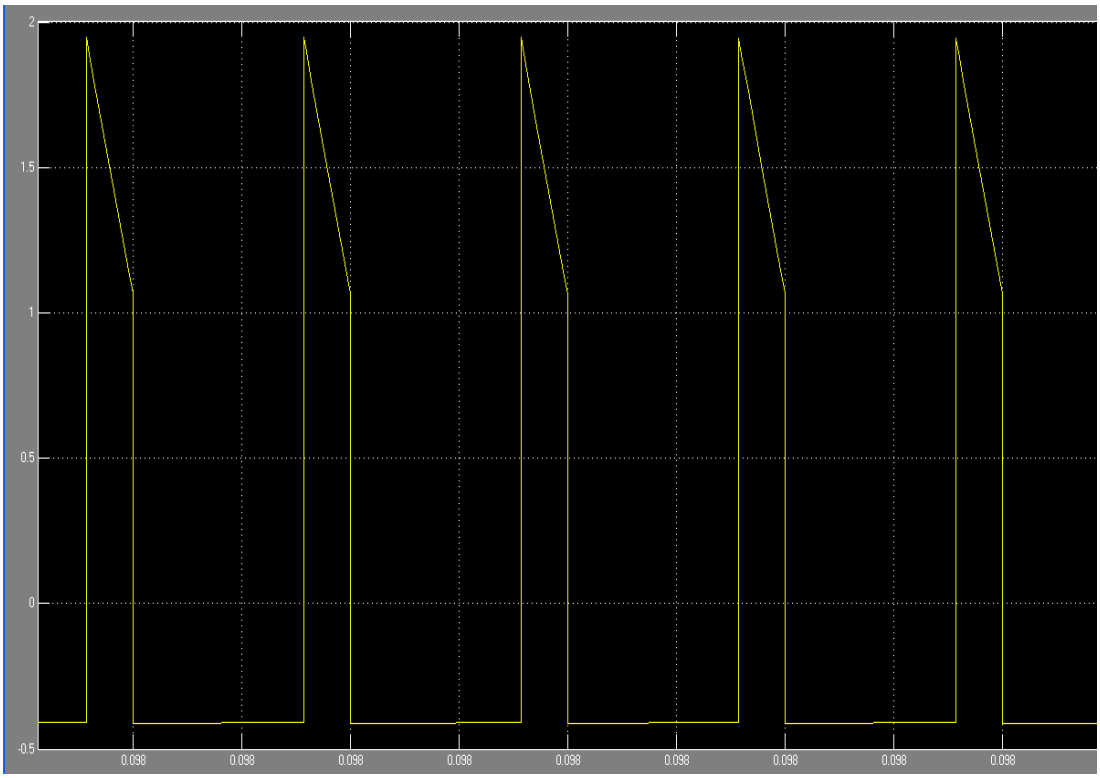

Figure 3.8: The Output Capacitor Current of Basic Converter Topology

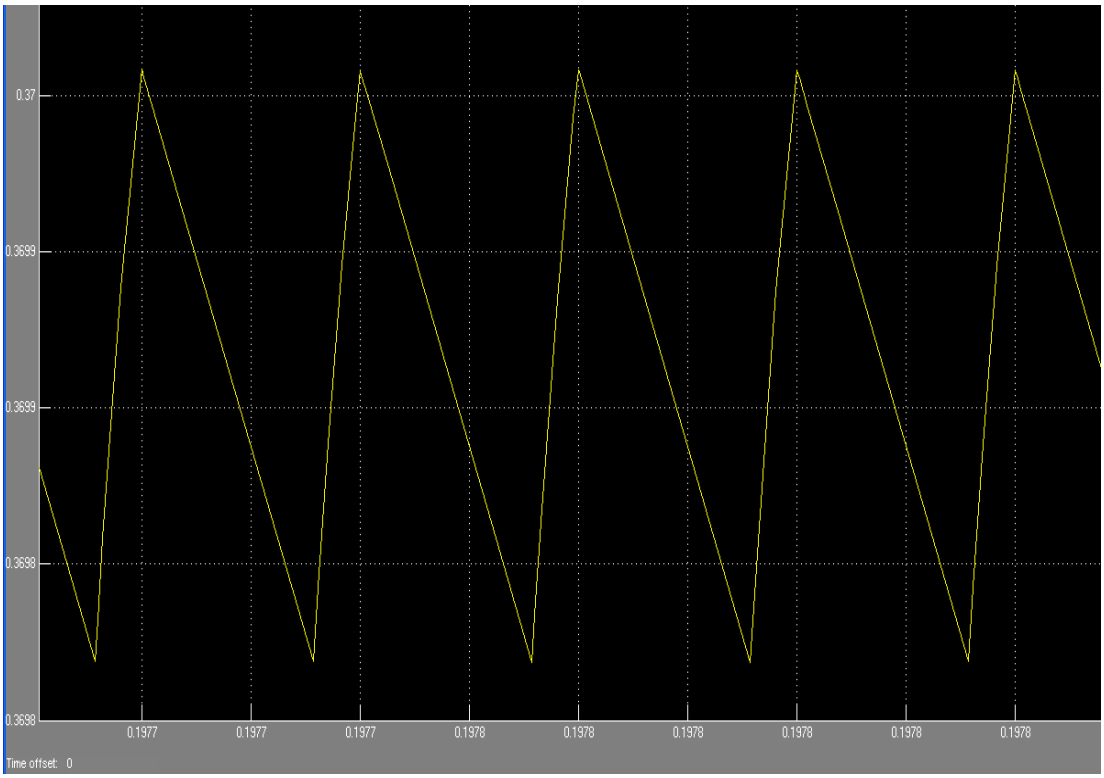

Figure 3.9: The Output Current of Basic Converter Topology

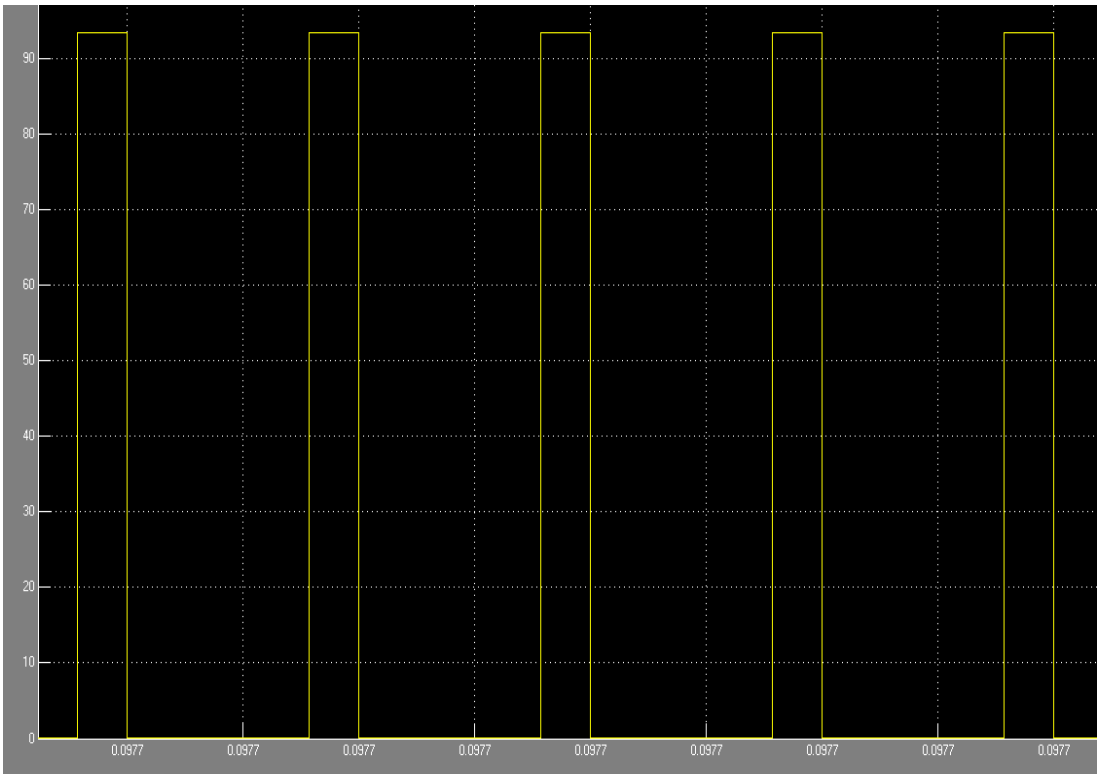

Figure 3.10: The Switch Voltage Stress of the Basic Converter Topology

From Figures 3.6 and 3.7 it's clearly shown the current value of the inductors $L_1$and L_2 are equal and with peak value approximately equal to 2.4 Ampere.

To find power output in accordance with Figures 3.4 and 3.9 the approximate value of V_o =92.54Vand the value of $I_o = 0.372$A by substitute these value in (3.23).

$$P_o = V_o I_o \tag{3.23}$$

$$P_o = (96.216)(\ 0.372) \approx 35.792\text{W}$$

Its mean there's power losses in the IGBT switch and in the diodes this power will decreases in the first improved topology moreover the voltage stress cross the IGBT switch V_{s1} in Figure 3.10 equal the output voltage V_o in Figure 3.4 the value of V_{s1} is

$$V_{s1} = V_o \approx 96.216\text{V}$$

The following sections discuss three improved transformerless boost converter topologies based on the latter one. They are proposed in [1].

3.3The First Improved Topology

Figure 3.11 shows the first improved topology. The improvement over the basic topology explained in section 3.1 is the increase in voltage gain as will be seen in this section.

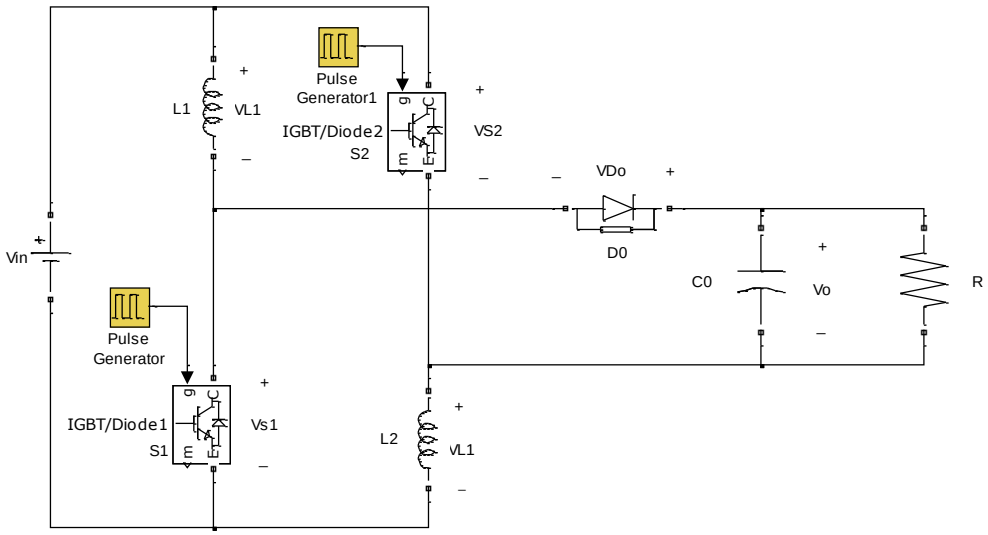

Figure 3.11: The First Improved Topology

Fig.3.11 shows the simulink model of the converter which consists of two active switches (S_1 and S_2), two equal inductors (L_1 and L_2 of 100μH), one output diode(D_0) ,one output capacitor(C_0 of 68 μF) and a resistance (R) of 250Ω. Switches S_1 and S_2 are IGBT switches which are controlled by using one control signal which is square pulse with amplitude 1V.

The operation of this converter includes two distinct modes; the continuous conduction mode (CCM) and the discontinuous mode (DCM) as depicted in Figure 3.12 which shows typical voltage and current waveforms of this topology during both modes.

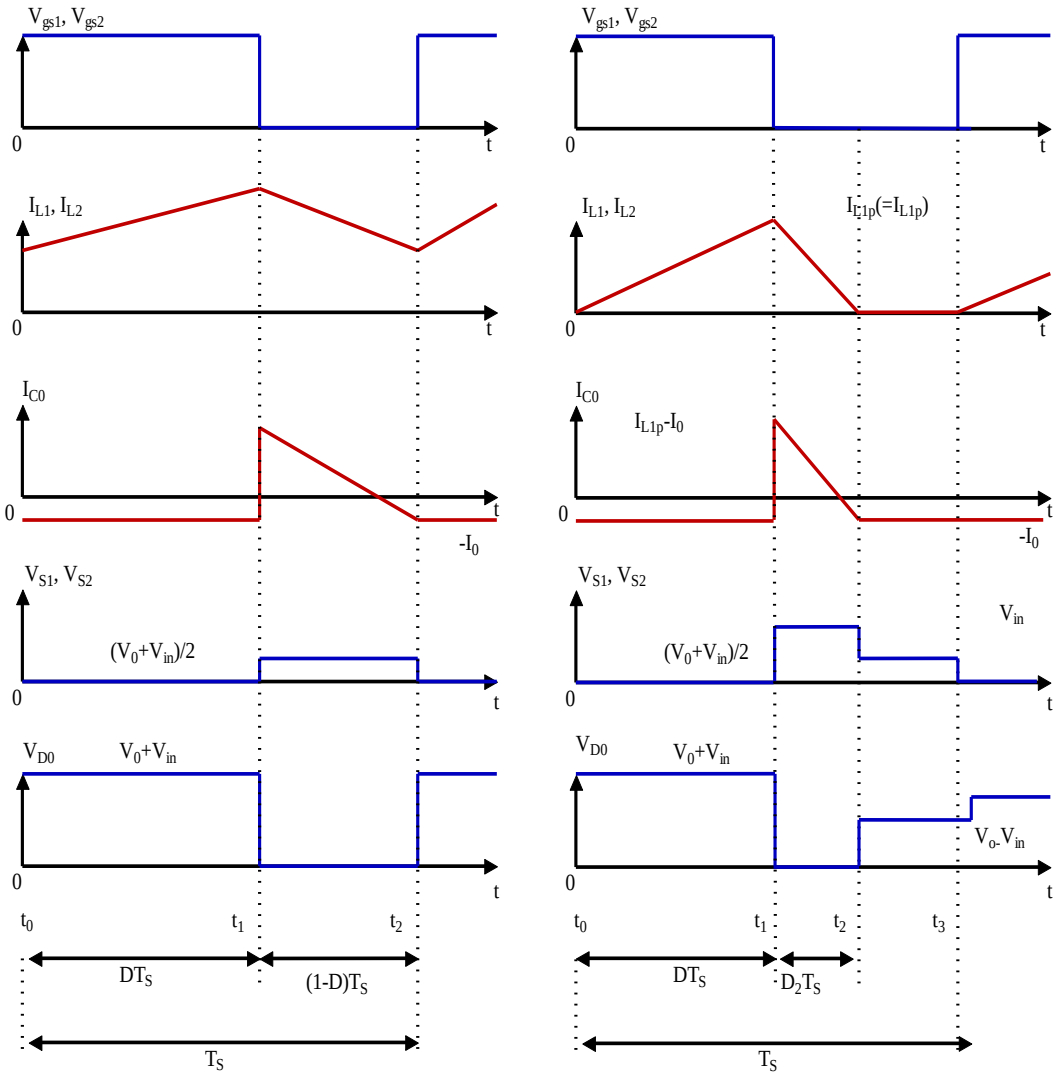

Figure 3.12: Typical Voltage and Current waveforms for the First Topology

3.3.1 The Continuous Conduction Mode (CCM)

This mode of operation can be further divided into two stages:

Stage 1: this stage extends from t_0 to t_1 as sown in Figure 3.12-a. In this interval, switches S_1 and S_2 are both turned on, and the equivalent circuit of the converter will be as shown in Figure 3.13. During this stage, inductors L_1 and L_2 are charged in parallel from the DC source where as the capacitor stores energy to release it to the load.

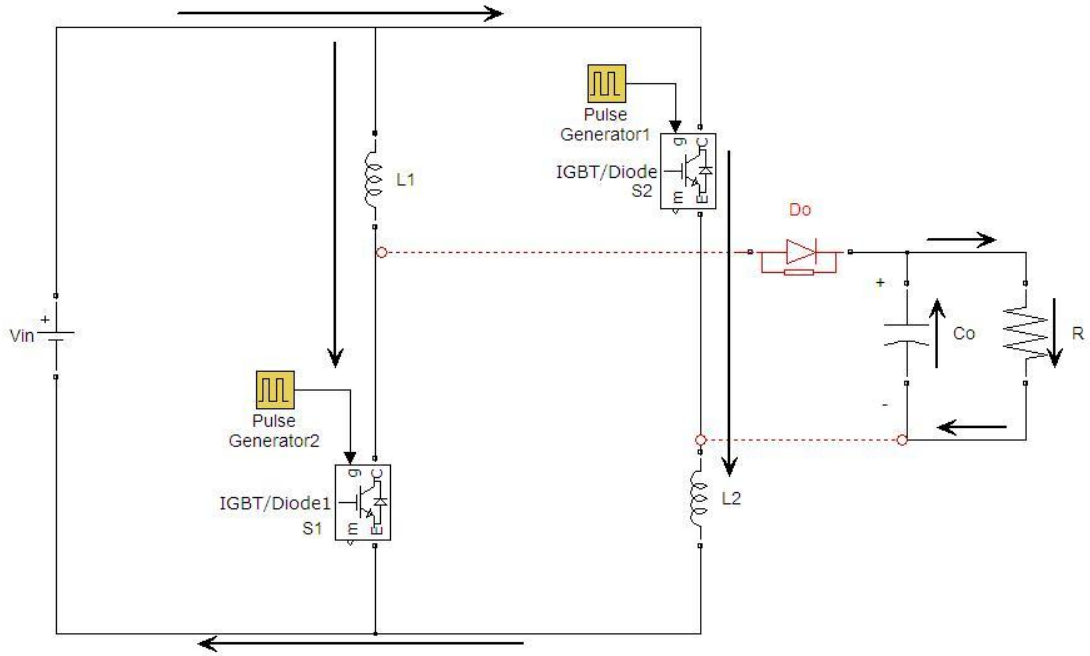

Figure 3.13: The Equivalent Circuit of CCM -stage 1 for the First Topology

Considering the circuit of Figure 3.13, the voltages of L_1 and L_2 are given by:

$$V_{L1} = V_{L2}=V_{in} \tag{3.24}$$

Stage 2: extends from t_1 to t_2 appearing in Figure 3.12-a.During this time interval, S_1 and S_2 are switched off as shown in the equivalent circuit shown in Figure 3.14. Besides, L_1 and L_2 are connected in series and the capacitor charges so that the load voltage equals the capacitor voltage. The result is that:

$$V_{in}- (V_{L1} +V_{L2})= V_o \tag{3.25}$$

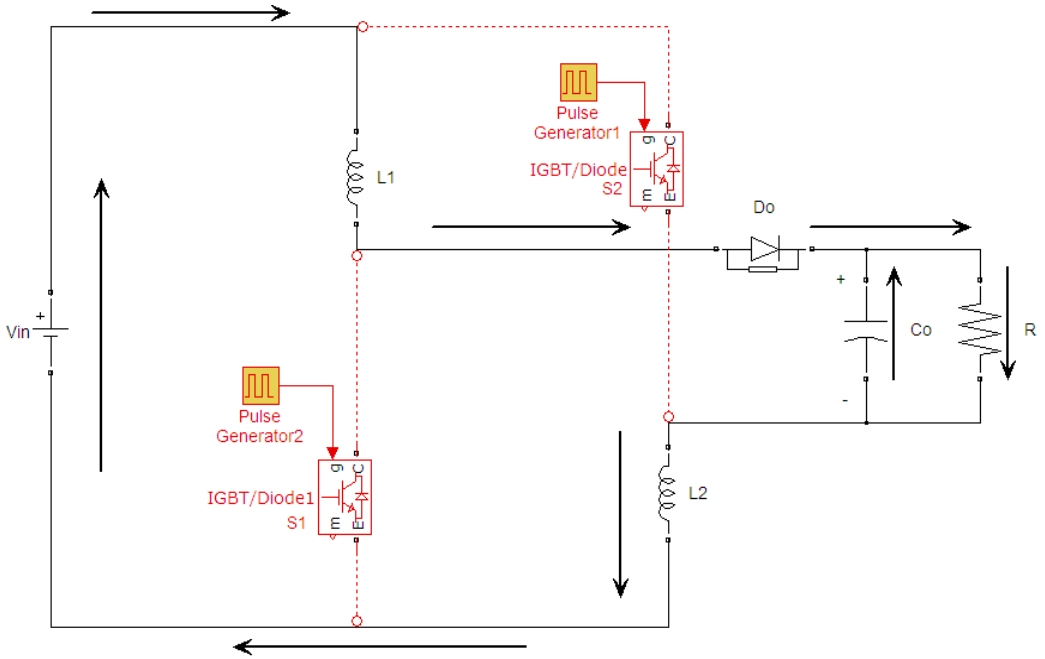

Figure 3.14: The Equivalent Circuit of CCM-stage 2 for the First Topology

Taking into consideration thatV_{L1} equalsV_{L2}, one can write:

$$V_{L1}=V_{L2}=\frac{V_{in}-V_o}{2} \tag{3.25}$$

The fact that the two inductors are equal in value and have the same current implies the condition in (3.26). Doing the integration in (3.26), the voltage gain can be evaluated as in (3.27).

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \frac{V_{in}-V_0}{2} dt = 0 \tag{3.26}$$

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \tag{3.27}$$

, where D is the duty cycle.

The voltage of the switches S_1 and S_2 in the interval $[DT_s,T_s]$is given by

$$\mathrm{V_{s1}} = \mathrm{V_{s2}} = \frac{V_o+V_{in}}{2} \tag{3.28}$$

Moreover, the diode voltage is

$$\mathrm{V_{DO}} = V_{in} + V_o \tag{3.29}$$

The voltage gain in (3.27) is plotted versus duty cycle (D) in Figure 3.15. Comparing the result obtained in this figure to that of basic circuit shown in Figure 3.3, the improvement in voltage gain with the first transformerless boost converter topology over that of the basic converter is notable by comparing the plots in Figures 3.3 and 3.15.

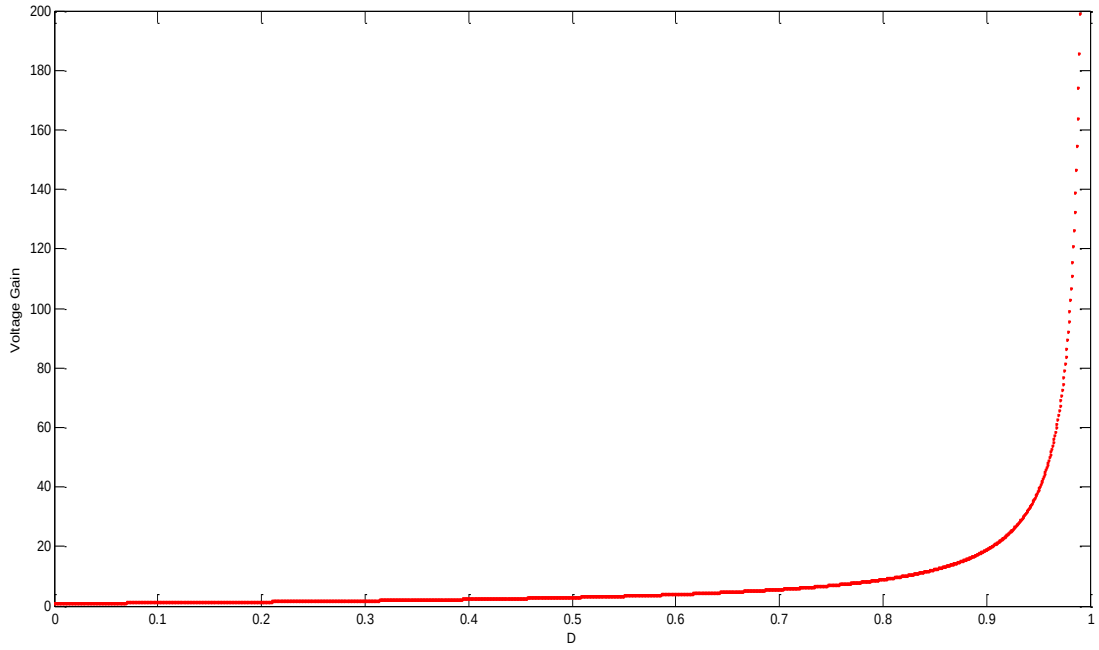

Figure 3.15: Voltage Gain versus Duty Cycle for the First Topology in the CCM for the First Topology

3.3.2 The Discontinuous Conduction Mode (DCM)

The DCM is also subdivided into three distinct stages:

stage1: which takes place between t_0 and t_1 appearing in Figure 3.12-b.During this time interval, the switches S_1 and S_2 are both switched on, the inductors L_1 and L_2 are charged in parallel from the DC source, so that the load voltage equals the capacitor voltage. Meanwhile, the capacitor stores energy to release it to the load. During this stage the converter will have the equivalent circuit shown in Figure 3.13.

Considering the circuit depicted in Figure 3.13, the inductor voltages and the input voltage are related by:

$$V_{L1}=V_{L2}=V_{in} \tag{3.30}$$

The currents passing through L_1 and L_2 at the end of the first stage are formulated as in (3.31) and (3.32), respectively.

$$I_{L1}=\frac{1}{L}\int_0^{DT_S} V_{in}\,dt \tag{3.31}$$

$$I_{L2}=\frac{1}{L}\int_0^{DT_S} V_{in}\,dt \tag{3.32}$$

Doing the integral in (3.31) and (3.32), and applying the condition of (3.30), the peak inductor currents are formulated as:

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_{in}}{L_{eq}} DT_s \tag{3.33}$$

,where L is the inductance which equals L_1 and L_2

Stage 2: which extends from t_1 to t_2 appearing in Figure 3.12-b.In this time interval, the switches S_1 and S_2 are turned off, the inductors L_1 and L_2 are series connected to the capacitor C_o which charges during this time, so the converter has the equivalent circuit shown in Figure 3.14.The inductor currents $\mathrm{I_{L1p}}$ and $\mathrm{I_{L2p}}$ start decreasing to zero at $t = t_2$. Another expression for $\mathrm{I_{L1p}}$and $\mathrm{I_{L2p}}$ is that of (34).

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_o - V_{in}}{2L}\, D_2 T_s \tag{3.34}$$

Stage 3: which occurs between t_2 and t_3 shown in Figure 3.12-b. During this time interval, S_1 and S_2 are still turned off, the capacitor charges the R-load and the energy in L_1 and L_2 is zero. The equivalent circuit of the converter during this stage is explained in Figure 3.16.

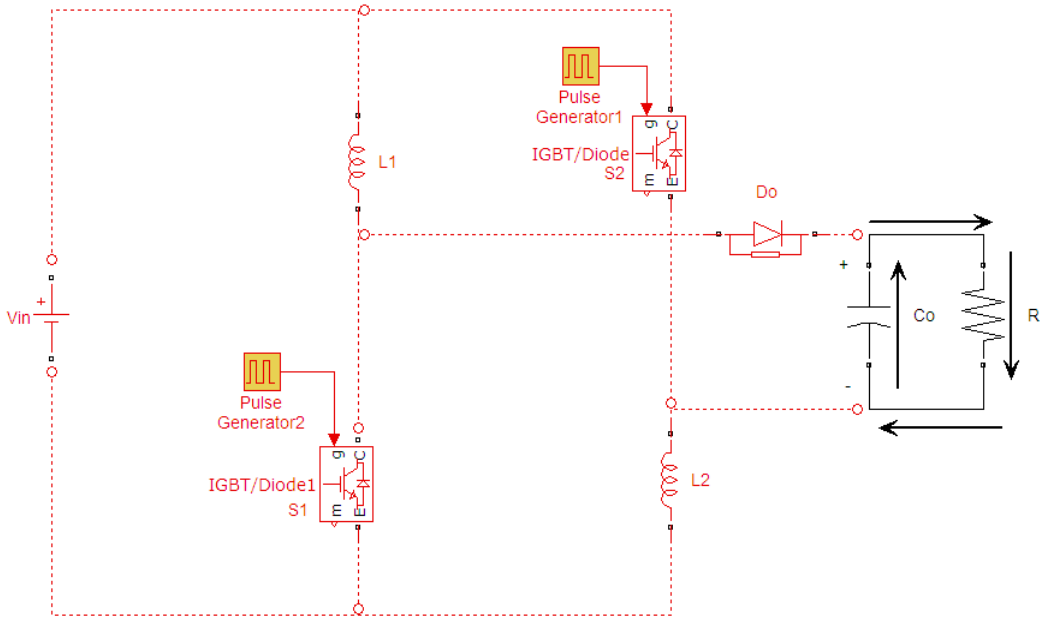

Figure 3.16: The Equivalent Circuit of DCM stage-3 for the First Topology

Rearranging (3.34) and substituting (3.33), one can write:

$$\mathrm{D_2} = \frac{2\mathrm{DV_{in}}}{V_o - V_{in}} \tag{3.35}$$

Observing the waveform of I_{Co} in Figure 3.12-b, the average value of the capacitor output current during the whole period is found as follows:

$$I_{Co} = \frac{\frac{1}{2}D_2 T_S \mathrm{I_{L1p}} - \mathrm{I_O T_S}}{\mathrm{T_S}} = \frac{1}{2} D_2 \mathrm{I_{L1p}} - \mathrm{I_o} \tag{3.36}$$

Substituting (3.33) and (3.35) in (3.36), the result is:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - V_{in})} - \frac{V_o}{R} \tag{3.37}$$

Under the steady state condition, the average capacitor output current equals zero, so:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - V_{in})} - \frac{V_o}{R} = 0 \tag{3.38}$$

, or equivalently:

$$\frac{V_o}{R} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - V_{in})} \tag{3.39}$$

Based on the aforementioned discussion, the normalized time constant of the inductor is:

$$\tau_L \equiv \frac{L f_s}{R} \tag{3.40}$$

, where $f_s = \frac{1}{T_S}$ is the switching frequency. Then, substituting (3.40) into (3.39), the voltage gain is given by:

$$\frac{V_o}{V_{in}} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{D^2}{\tau_L}} \tag{3.41}$$

Based on (3.41), Figure 3.17 shows the plot of the voltage gain versus duty cycle in the discontinuous mode. Clearly, the gain approximately equals 1 meaning that the output voltage equals the input voltage. This result is due to the relatively large time constant of the inductors as the values used for this plot were: $L_1 = L_2$=100μH and $f_s = 100KHz$.

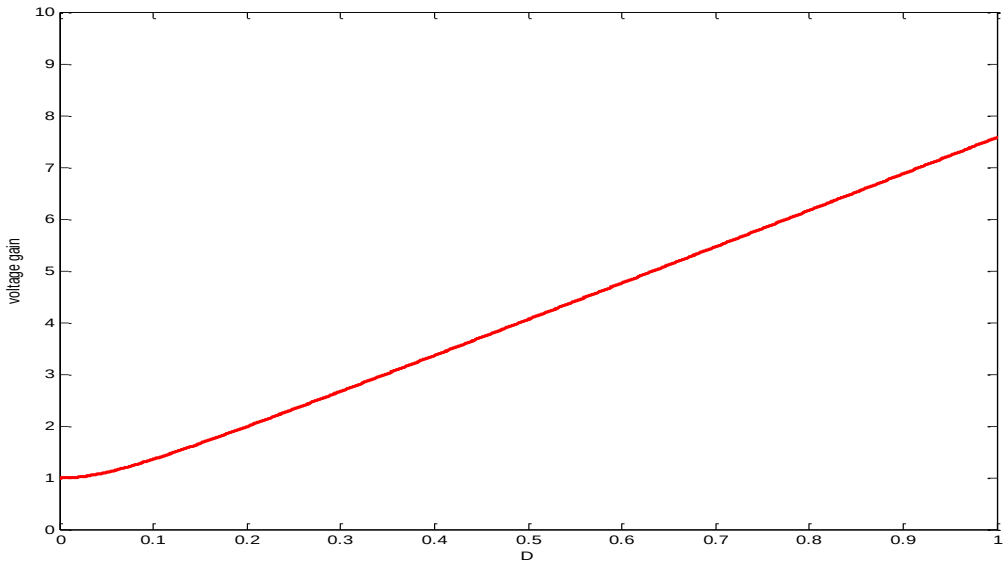

Figure 3.17: Voltage Gain versus Duty Cycle for the First Topology in the DCM for the First Topology

3.3.3 Boundary Operating Condition between CCM and DCM

The converter being discussed in this section can operate on a boundary (margin) between the DCM and the CCM. The inductor time constant for such a boundary can be derived by equating the voltage gains of the CCM and DCM modes appearing in (3.27) and (3.41), respectively to be as in (3.43). Figure 3.18 shows a plot of τ_{LB} versus D.

$$\tau_{LB} = \frac{D(1-D)^2}{2(1+D)} \tag{3.43}$$

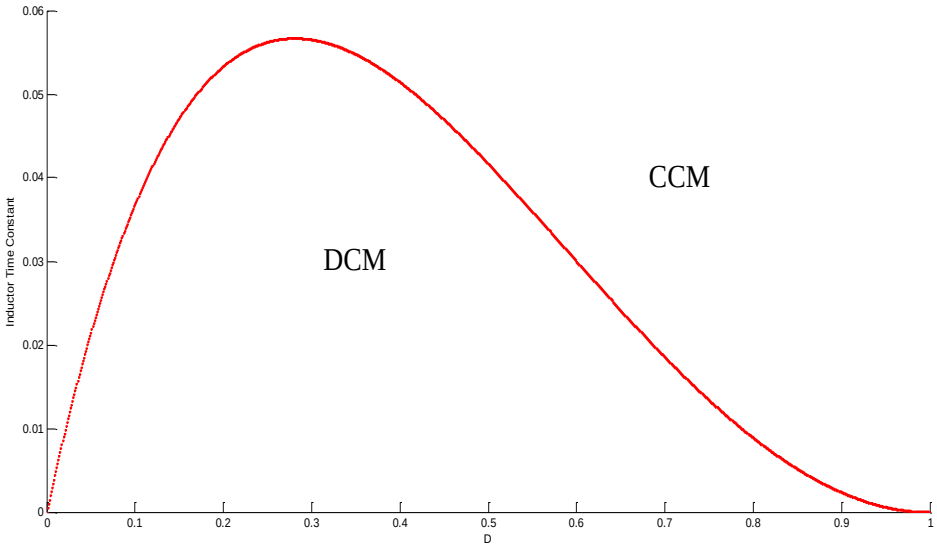

Figure 3.18: Inductor Time Constant versus Duty Cycle for the First Topology in the Boundary Mode

3.4 Calculations and Simulation Results of the First Improved Topology

This section carry simulation result of the first improved topology Figure .3.11 by using MATLAB Simulink. From the reference [1] the parameter values that are used are: L_1=L_2 =100μH , P_o= 40W , $V_{IN} = 12V$, $V_o = 100V$ and C_o=68μF , f_s=100KHz The load resistance R_O=250 Ω and the duty cycle D is obtained by using equation (3.25).

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} = \frac{100}{12} \tag{3.44}$$

D=0.7857= 78.57%

Figure 3.19 shows the output voltage V_o and Figure 3.20 shows V_{DO} and also Figure 3.21 and Figure 3.22 shows the current during inductors $I_{L1}, I_{L2}$and Figure3.23 the current passed in the output capacitor I_{Co} and Figure 3.24 shows the output current $I_o$finally Figure 3.25and Figure 3.26 delivers voltage switches stress $V_{s1}$and V_{s2}.

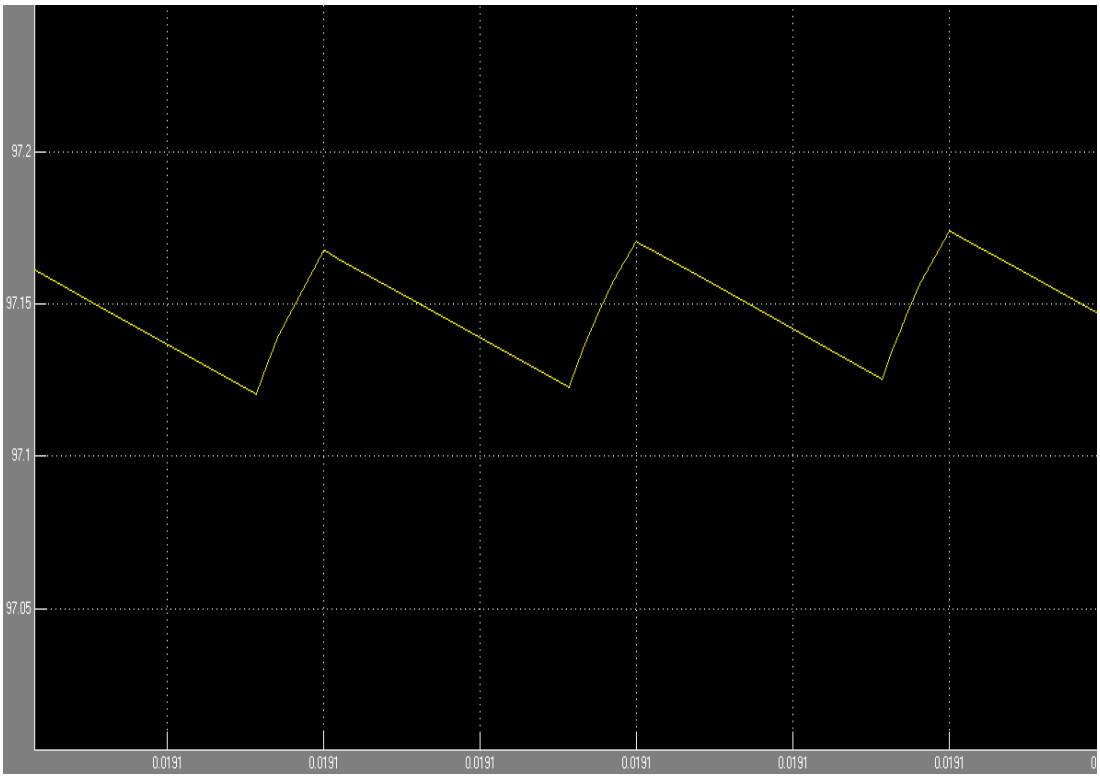

Figure 3.19 The Output Voltage of First Improved Topology

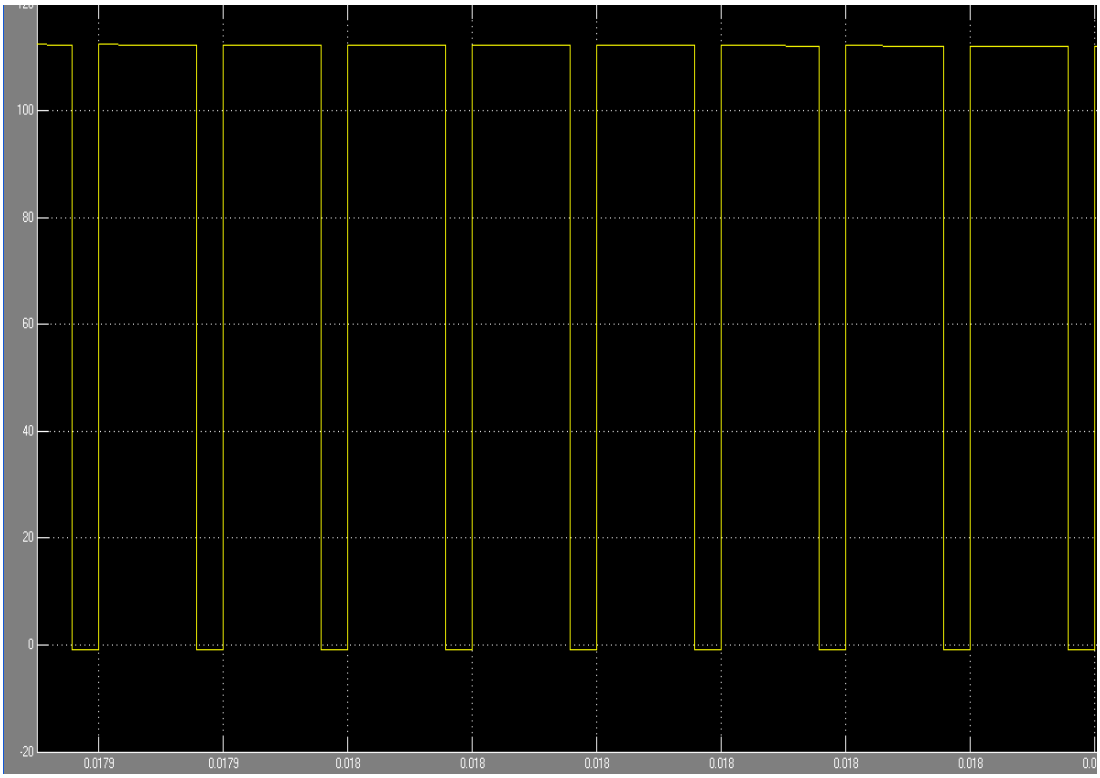

Figure 3.20: The Diode Voltage of First Improved Topology

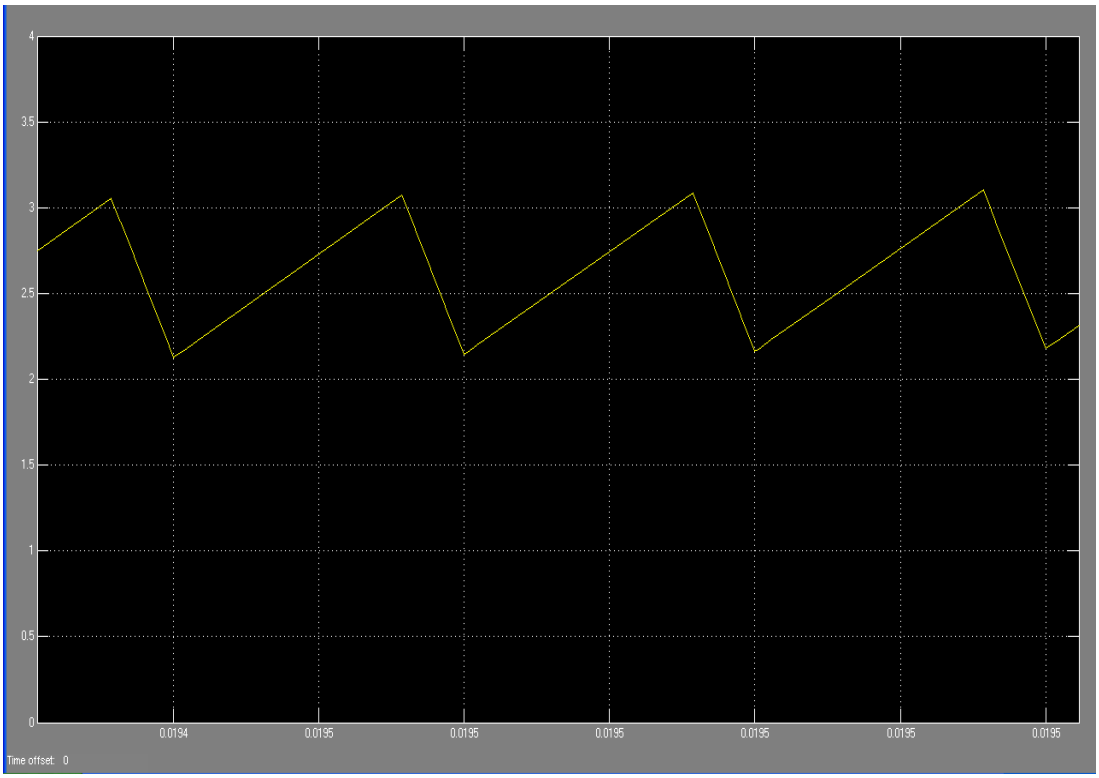

Figure 3.21: The L_1 Current of First Improved Topology

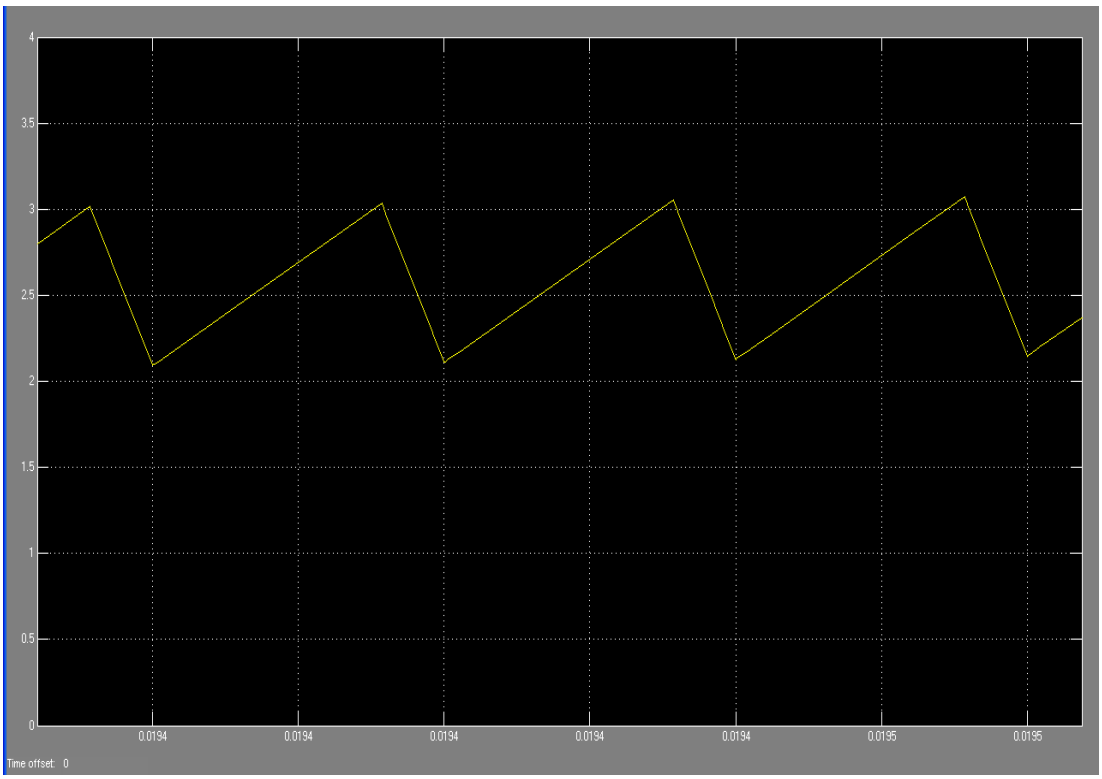

Figure 3.22: The L_2 Current of First Improved Topology

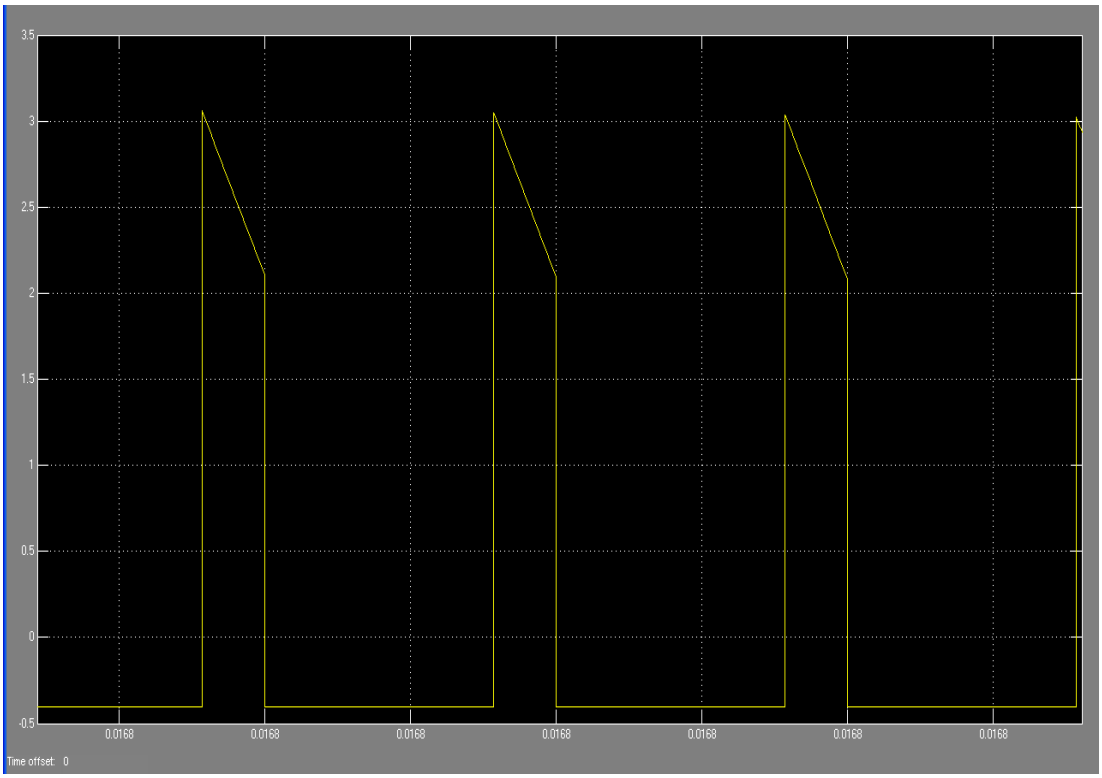

Figure 3.23: The Output Capacitor Current of First Improved Topology

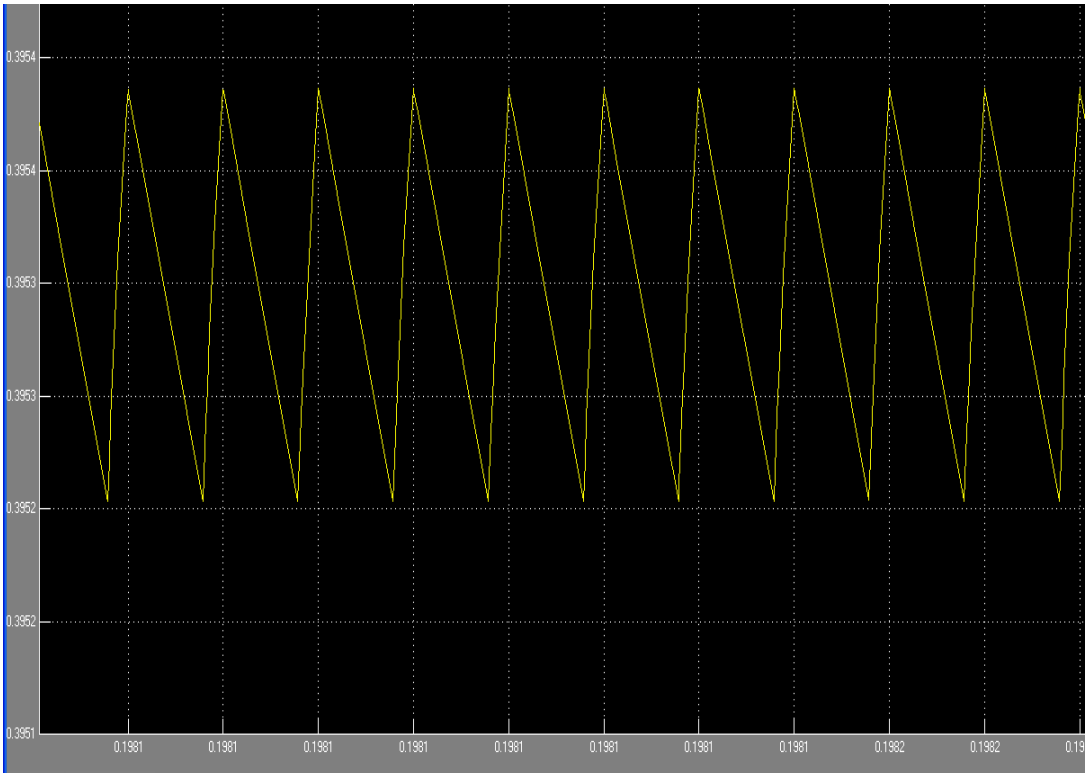

Figure 3.24:The Output Current of Basic First Improved Topology

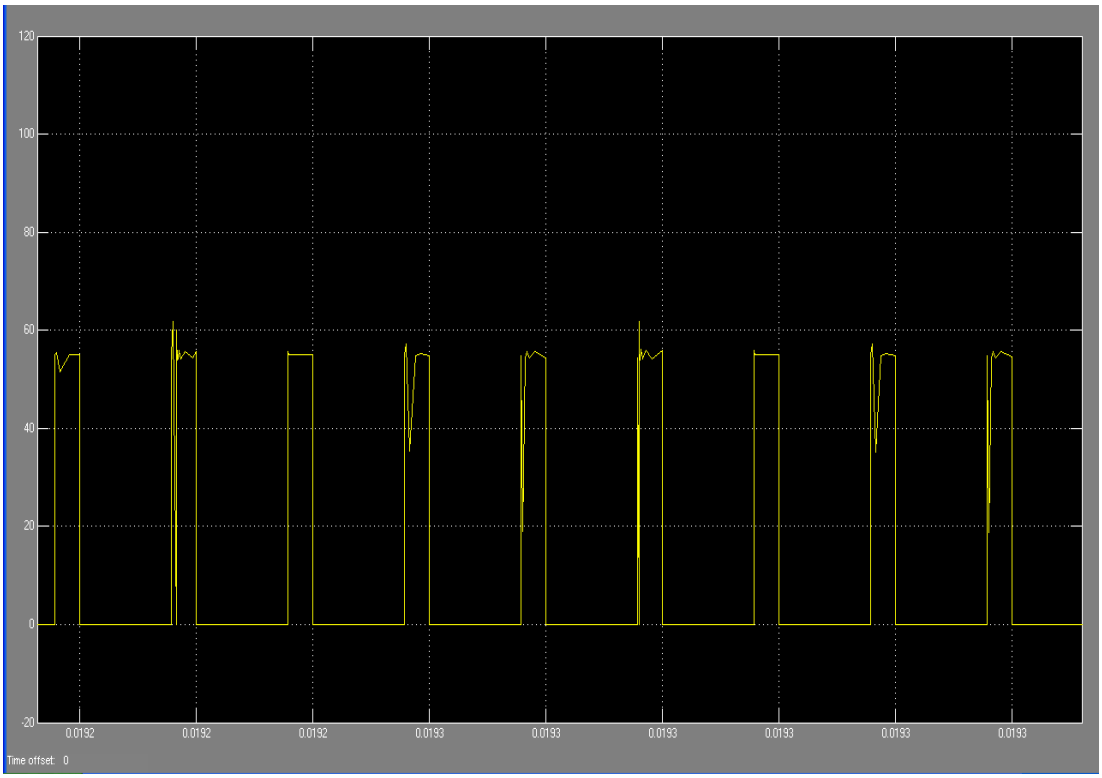

Figure 3.25: The Switch Voltage Stress V_{S1} of the First Improved Topology

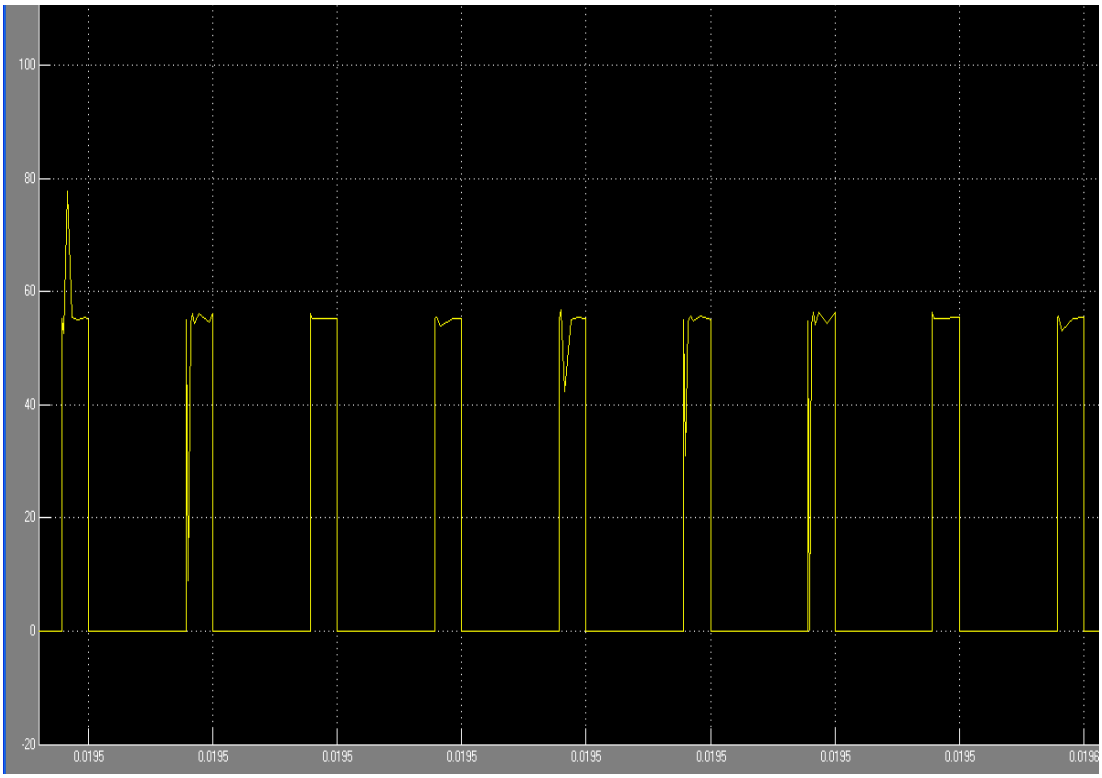

Figure 3.26: The Switch Voltage Stress V_{S2} of the First Improved Topology

From Figures 3.21 and 3.22 it is clearly shown the current value of the inductors $L_1$and L_2 are equal and it's approximately equal 3 ampere .and from Figure 3.23 the value of the current C_o approximately equal.

$$I_{Co} = \mathrm{I_{L1}} - \mathrm{I_o} \approx 2.7\mathrm{A} \tag{3.45}$$

To find power output in accordance with Figures 3.19 and 3.24 the approximate value of $V_o \approx$ 97.1525Vand the value of $\mathrm{I_o} \approx$ 0.3887A by substuited these value in this formula (3.46).

$$P_o = V_o I_o \tag{3.46}$$

$$P_o = (97.1525)(\ 0.3954) \approx 38.414\mathrm{W}$$

By comparing the value of the power output in this topology with the basic topology the first improve topology raised the power output and the voltage gain it is mean the power losses and the voltage stress cross two IJBT switches decrease and the value of the voltage stress $V_{s1}$and V_{s2} are equal its clearly shown in Figures 3.25and 3.26 to obtaining these values using formula (3.28).

$$V_{s1} = V_{s2} = \frac{(97.1525+12)}{2} \approx 54.576\mathrm{V}$$

3.5The Second Improved Topology

This topology is the same as the first one except for adding capacitor (C_1) and diode (D_1) which are parallel to inductance L_1. Inductances L_1 and L_2 have the same values. Moreover, switches S_1 and S_2 are IGBT switches and controlled by one control signal which is a square pulse with amplitude 1V. This topology is shown in Figure 3.27.

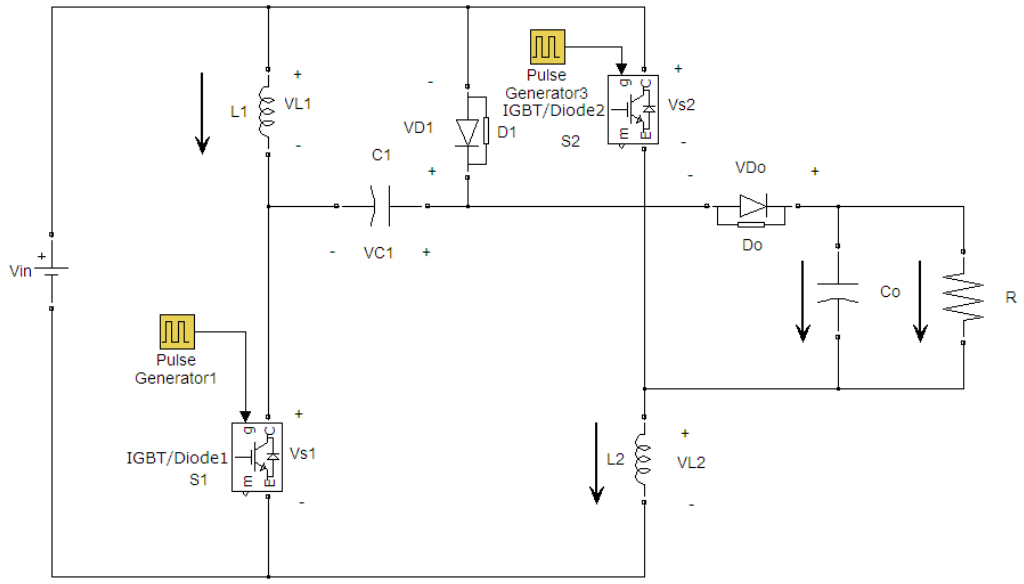

Figure 3.27: The Second Improved Topology

Fig.3.27 shows the simulink model of the converter which contains two active switches (S_1 and S_2), two equal inductors (L_1 and L_2 of $100\mu H$), one output diode(D_0) ,two capacitors (C_0 of 68 μF) and(C_1 of $57\mu F$) and a resistance (R) of 250Ω. Switches S_1 and S_2 are IGBT switches which are controlled by using one control signal which is square pulse with amplitude 1V.

The operation of this converter includes two distinct modes; the continuous conduction mode (CCM) and the discontinuous mode (DCM) as depicted in Figure 3.28 which shows typical voltage and current waveforms of this topology during both modes.

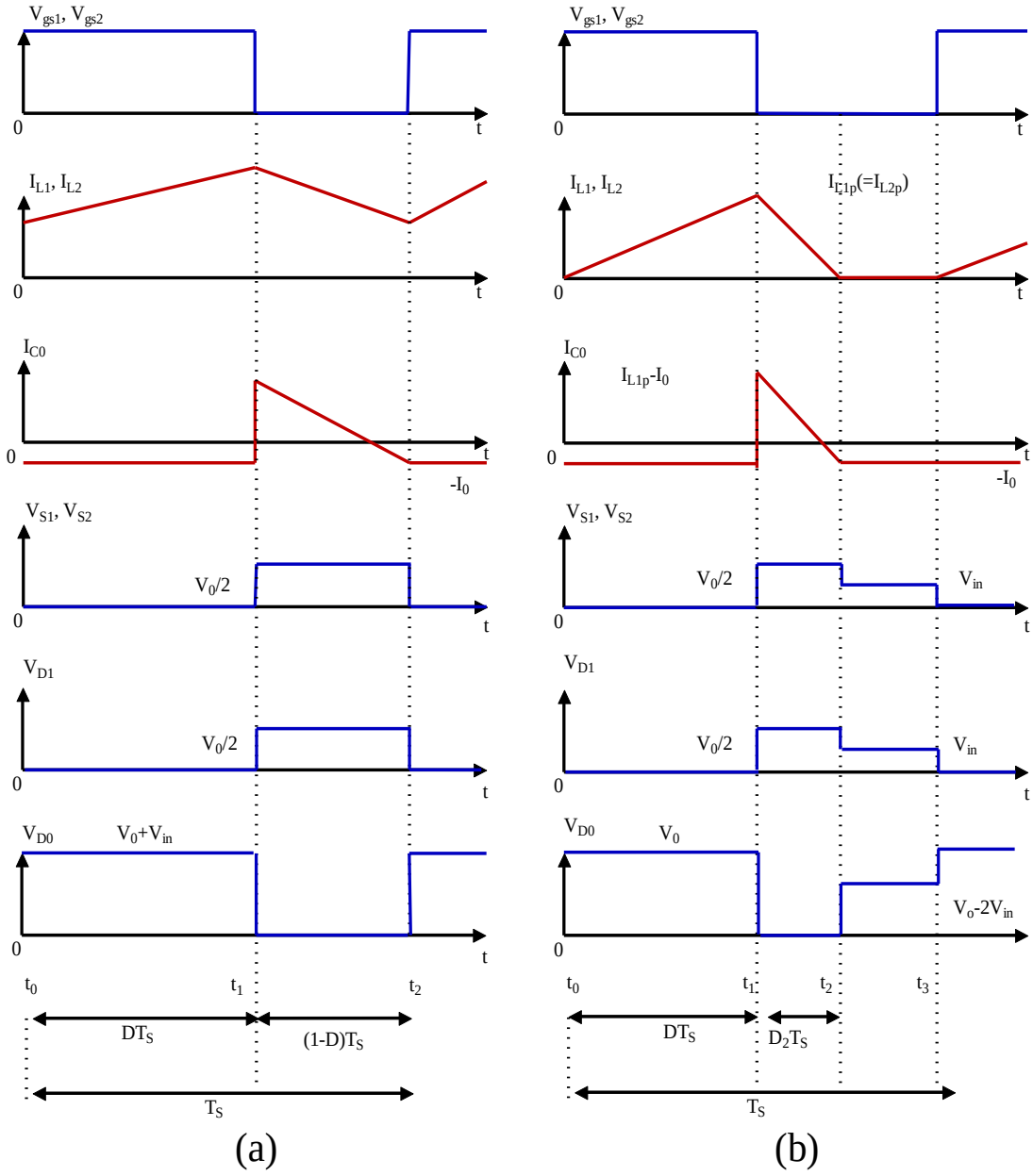

Figure 3.28: Typical Voltage and Current waveforms for the Second Topology

3.5.1 The Continuous Conduction Mode (CCM)

This mode of operation can be further divided into two stages:

Stage 1: This stage extends from t_0 to t_1 as sown in Figure 3.28-a. In this interval, switches S_1 and S_2 are both turned on, and the equivalent circuit of the converter is as shown in Figure 3.29. During this stage, inductors L_1 and L_2 are charged in parallel from the DC source, whereas the capacitor C_o stores energy to release it to the load. Moreover, capacitor C_1 is charged from the DC source.

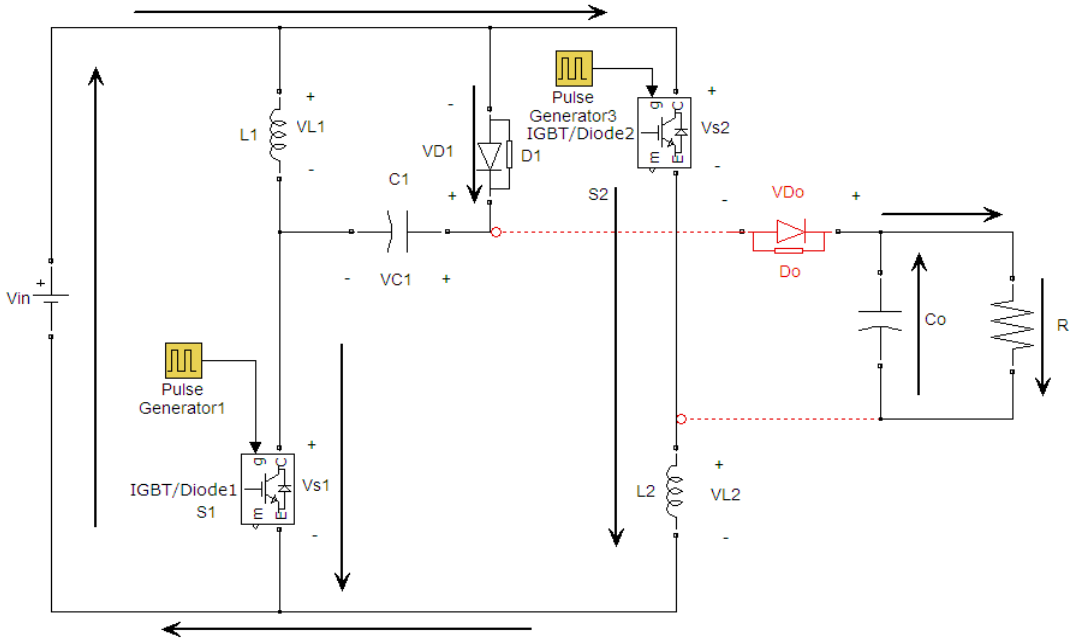

Figure 3.29: The Equivalent Circuit of CCM -stage 1 of the Second Topology

Considering the circuit of Figure 3.29, the voltages across L_1 , L_2 and C_1 are given by:

$$V_{L1} = V_{L2} = V_{in} = V_{C1} \tag{3.48}$$

Stage 2: extends from t_1 to t_2 appearing in Figure 3.28-a. During this time interval, S_1 and S_2 are switched off as shown in the equivalent circuit in Figure 3.30. Besides, L_1 , $C_1$and L_2 are connected in series to transfer the energy to C_o and the load. So, the voltages across L_1 and L_2 are derived as:

$$V_{L1} = V_{L2} = \frac{V_{in}+V_{C1}-V_o}{2} = \frac{2V_{in}-V_o}{2} \tag{3.49}$$

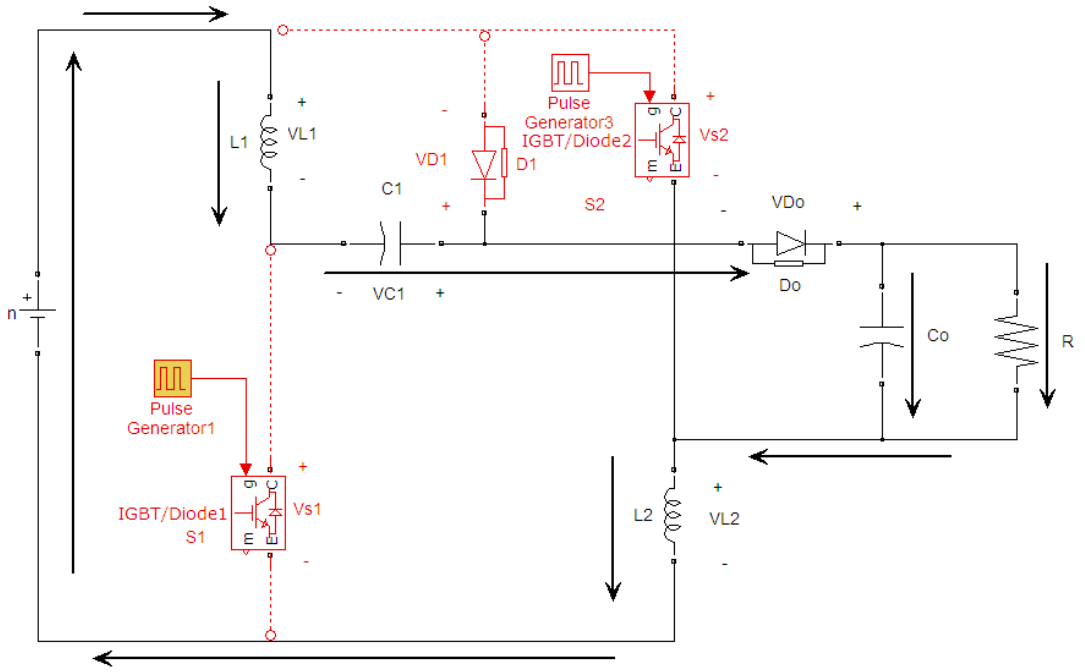

Figure 3.30: The Equivalent Circuit of CCM-stage 2 of the Second Topology

The fact that the two inductors are equal in values and have the same current implies the condition in (3.50). Doing the integration in (3.50), the voltage gain can be evaluated.

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \frac{2V_{in}-V_0}{2} dt = 0 \tag{3.50}$$

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{3.51}$$

, where, D is the duty cycle. The voltage of the switches S_1 and S_2 is given by

$$\mathrm{V_{s1}} = \mathrm{V_{s2}} = \mathrm{V_{D1}} = \frac{V_o}{2} \tag{3.52}$$

Moreover, the diode voltage is

$$\mathrm{V_{DO}} = V_o \tag{3.53}$$

The voltage gain in (3.52) is plotted versus duty cycle (D) in Figure 3.31. Comparing the result obtained in this figure to that of the first proposed topology shown in Figure 3.15, the improvement in voltage gain with the second transformerless boost converter topology over that of the first one is notable.

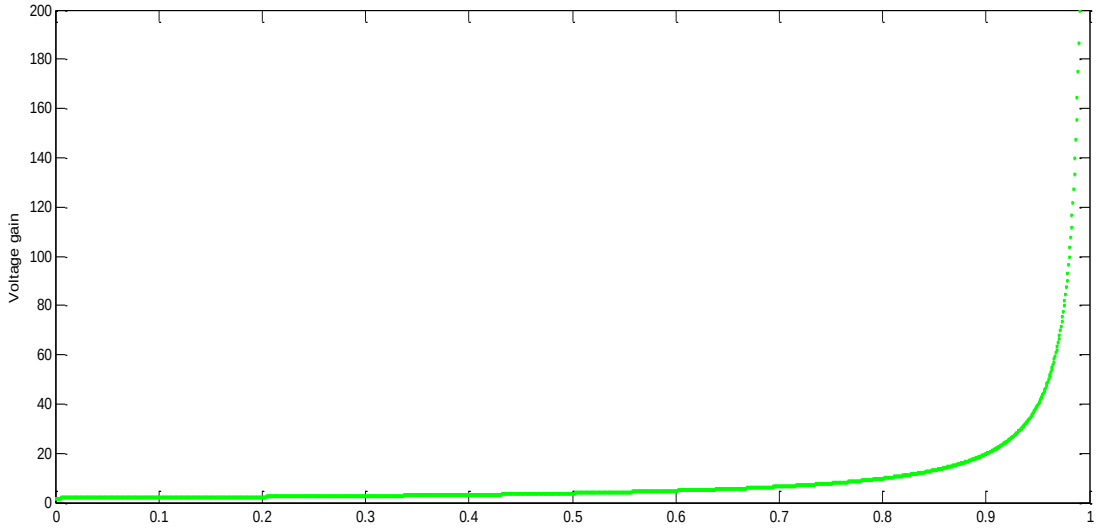

Figure 3.31: Voltage Gain versus Duty Cycle for the First Topology in the CCM of the Second Topology

3.5.2 The Discontinuous Conduction Mode (DCM)

The DCM is also subdivided into three distinct stages:

stage1: which takes place between t_0 and t_1 appearing in Figure 3.28-b.During this time interval, the switches S_1 and S_2 are both switched on, the inductors L_1 and L_2 are charged in parallel from the DC source. Moreover energy is stored in Co and C1 charges from the DC source, so that the load voltage equals the voltage of capacitor Co. Meanwhile, the capacitor Co stores energy to release it to the load. During this stage the converter will have the equivalent circuit shown in Figure 3.29.

Considering the circuit depicted in Figure 3.32, the inductor voltages and the input voltage are related by:

$$V_{L1}=V_{L2}=V_{in} \tag{3.54}$$

The currents passing through L_1 and L_2 at the end of stage 1 are formulated as in (3.55) and (3.56), respectively.

$$I_{L1}=\frac{1}{L}\int_0^{DT_S} V_{in}\,dt \tag{3.55}$$

$$I_{L2}=\frac{1}{L}\int_0^{DT_S} V_{in}\,dt \tag{3.56}$$

Doing the integral in (3.55) and (3.56), and applying the condition of (3.54), the peak inductor currents are formulated as:

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_{in}}{L_1} DT_s \tag{3.57}$$

Where L is the inductance which equals L_1 and L_2.

Stage 2: which extends from t_1 to t_2 appearing in Figure 3.28-b.In this time interval, the switches S_1 and S_2 are turned off, the inductors L_1 and L_2 and capacitor C1 are series connected to the capacitor C_o which charges during this time, so the converter has the equivalent circuit shown in Figure 3.30.The inductor currents $\mathrm{I_{L1p}}$ and $\mathrm{I_{L2p}}$ start decreasing to zero at $t = t_2$. Another expression for $\mathrm{I_{L1p}}$and $\mathrm{I_{L2p}}$ is that of (3.51).

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_o - V_{in} - V_{C1}}{2L} D_2 T_s = \frac{V_o - 2V_{in}}{2L} \tag{3.58}$$

Stage 3: which occurs between t_2 and t_3 shown in Figure 3.28-b. During this time interval, S_1 and S_2 are still turned off, the capacitor Co charges the R-load and the energy in L_1 and L_2 is zero. The equivalent circuit of the converter during this stage is explained in Figure 3.32.

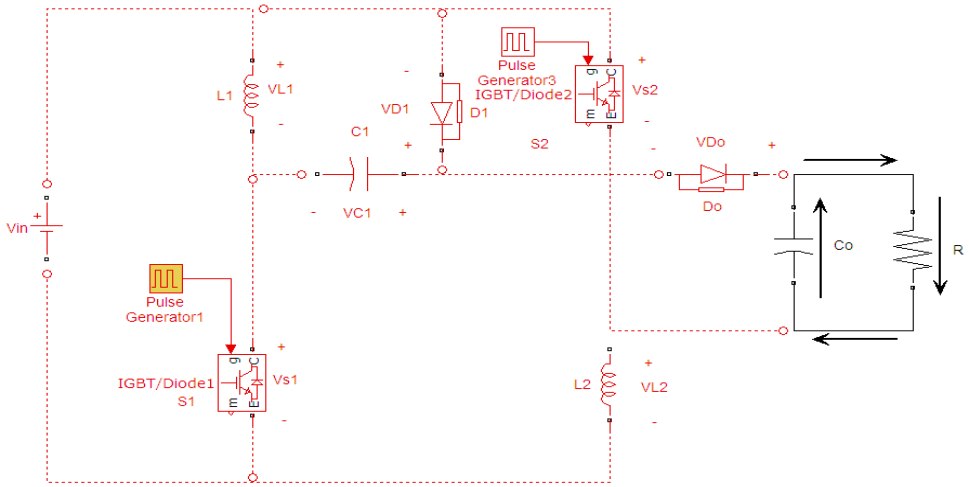

Figure 3.32: The Equivalent Circuit of DCM stage-3 of the Second Topology

Rearranging (3.58) and substituting (3.57), one can write:

$$\mathrm{D}_2 = \frac{2\mathrm{DV_{in}}}{V_o - 2V_{in}} \tag{3.59}$$

Observing the waveform of I_{Co} in Figure 3.28-b, the average value of the capacitor output current during the whole period is found as follows:

$$I_{Co} = \frac{\frac{1}{2}D_2 T_S \mathrm{I_{L1p}} - \mathrm{I_O T_S}}{\mathrm{T_S}} = \frac{1}{2} D_2 \mathrm{I_{L1p}} - \mathrm{I_o} \tag{3.60}$$

Substituting (3.58) and (3.59) in (3.60), the result is:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - V_{in})} - \frac{V_o}{R} \tag{3.61}$$

Under the steady state condition, the capacitor output current equals zero, so:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - 2V_{in})} - \frac{V_o}{R} = 0 \tag{3.62}$$

, or equivalently:

$$\frac{V_o}{R} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - 2V_{in})} \tag{3.63}$$

Based on the aforementioned discussion, the normalized time constant of the inductor is:

$$\tau_L \equiv \frac{L f_s}{R} \tag{3.64}$$

, where $f_s = \frac{1}{T_S}$ is the switching frequency. Then, substituting (3.64) into (3.63), the voltage gain is given by:

$$\frac{V_o}{V_{in}} = 1 + \sqrt{1 + \frac{D^2}{\tau_L}} \tag{3.65}$$

Based on (3.65), Figure 3.33 shows the plot of the voltage gain versus duty cycle in the discontinuous mode. Clearly, the gain approximately equals 1 meaning that the output voltage equals the input voltage. This result is due to the relatively large time constant of the inductors as the values used for this plot were:

$L_1 = L_2$=100μH and $f_s = 100KHz$

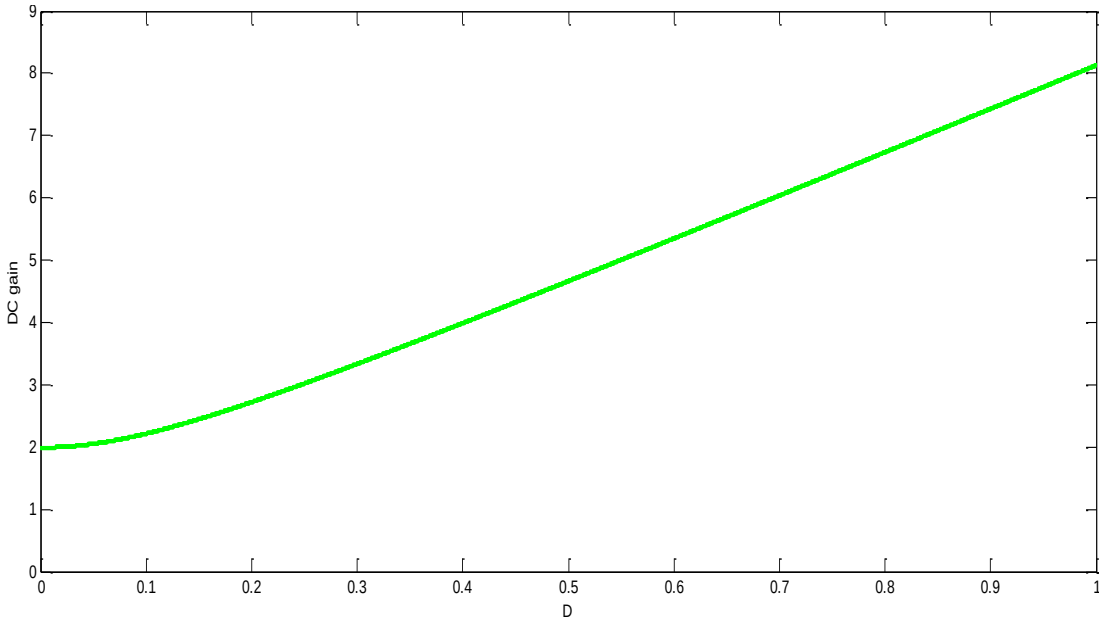

Figure 3.33: Voltage Gain versus Duty Cycle for the Second Topology in the DCM of the Second Topology

3.5.3 Boundary Operating Condition between CCM and DCM

The converter being discussed in this section can operate in a boundary between the DCM and the CCM. The inductor time constant for such a boundary can be derived by equating the voltage gains of the CCM and DCM modes appearing in (3.51) and (3.65), respectively to be as in (3.66). Figure 3.34 shows a plot of τ_{LB} versus D.

$$\tau_{LB} = \frac{D(1-D)^2}{4} \tag{3.66}$$

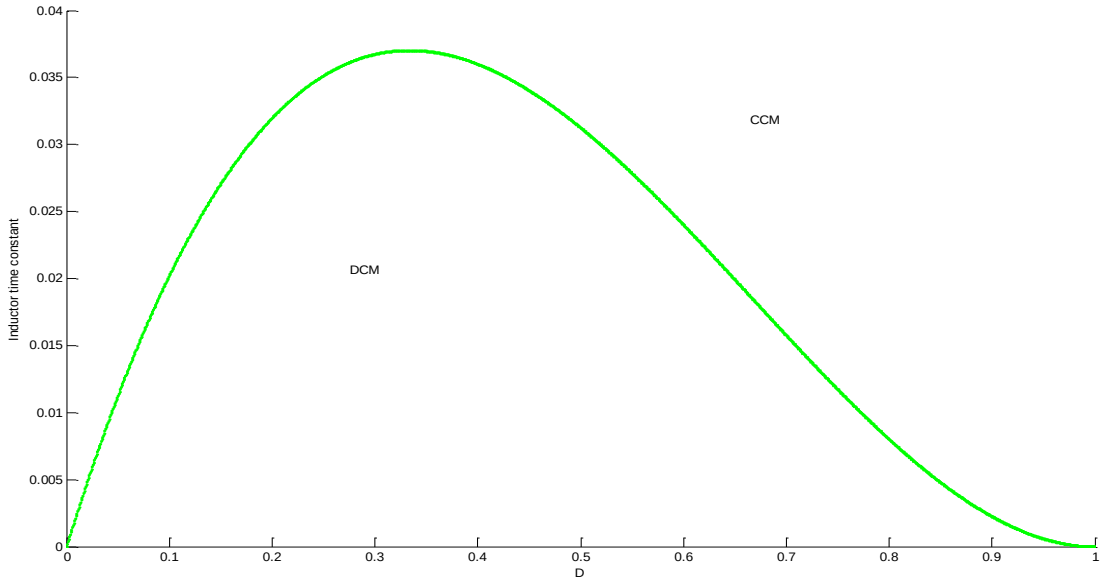

Figure 3.34: : Inductor Time Constant versus Duty Cycle for the First Topology in the Boundary Mode of the Second Topology

3.6 Calculations and Simulation Results of the Second Improved Topology

This section will present simulation results of the second improved topology Figure 3.27 by using MATLAB Simulink. From reference [1] the values that are used are: L_1=$L_{2=}$100μH , P_o= 40W , $V_{IN} = 12V$, $V_o = 100V$ and $C_1 = 57\mu F$ *and* C_o=68μF , f_s=100KHz and , R_o=250 Ω. To find the duty cycle D using the formula (3.51)

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} = \frac{100}{12} \tag{3.67}$$

D=0.76= 76%

Figure 3.35 shows the output voltage V_o and Figure3.36 shows V_{DO} and also Figure 3.37 and Figure 3.38 show the current in inductors I_{L1}, I_{L2} and Figure3.39 the current in the output capacitor I_{Co} and figure 3.40 shows the output current $I_o$finally Figures 3.41 and 3.42 delivered voltage switch stresses $V_{s1}$and V_{s2}, respectively.

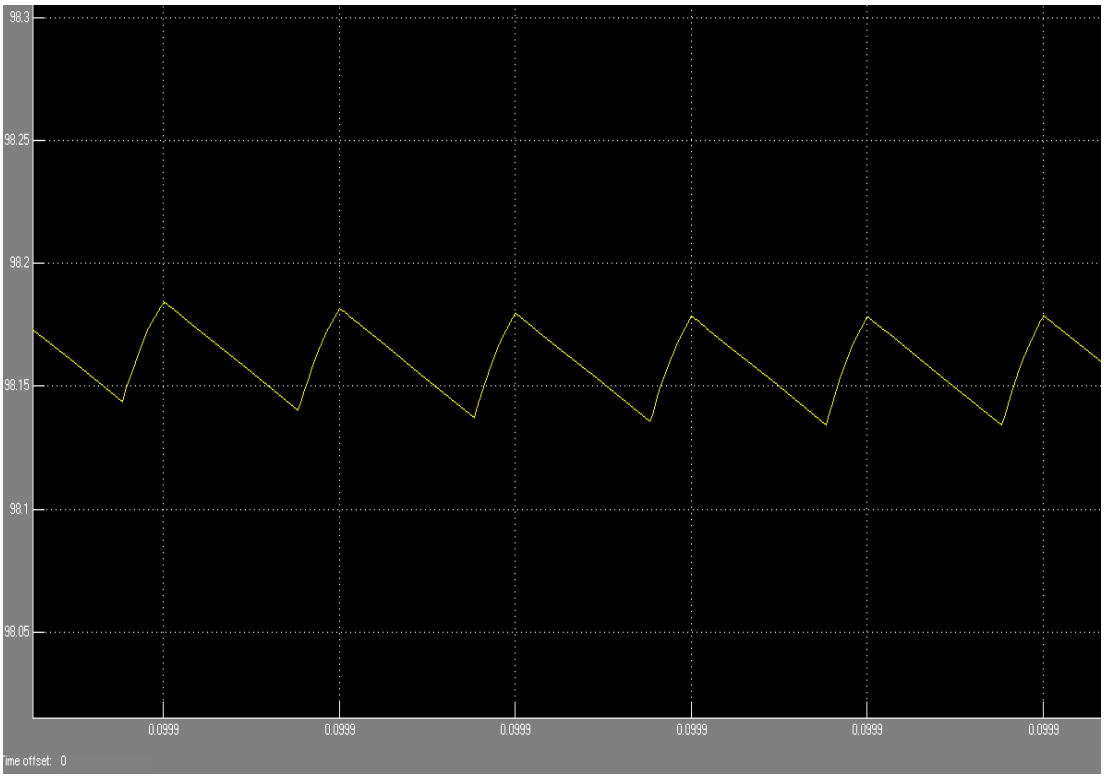

Figure 3.35: The Output Voltage of Second Improved Topology

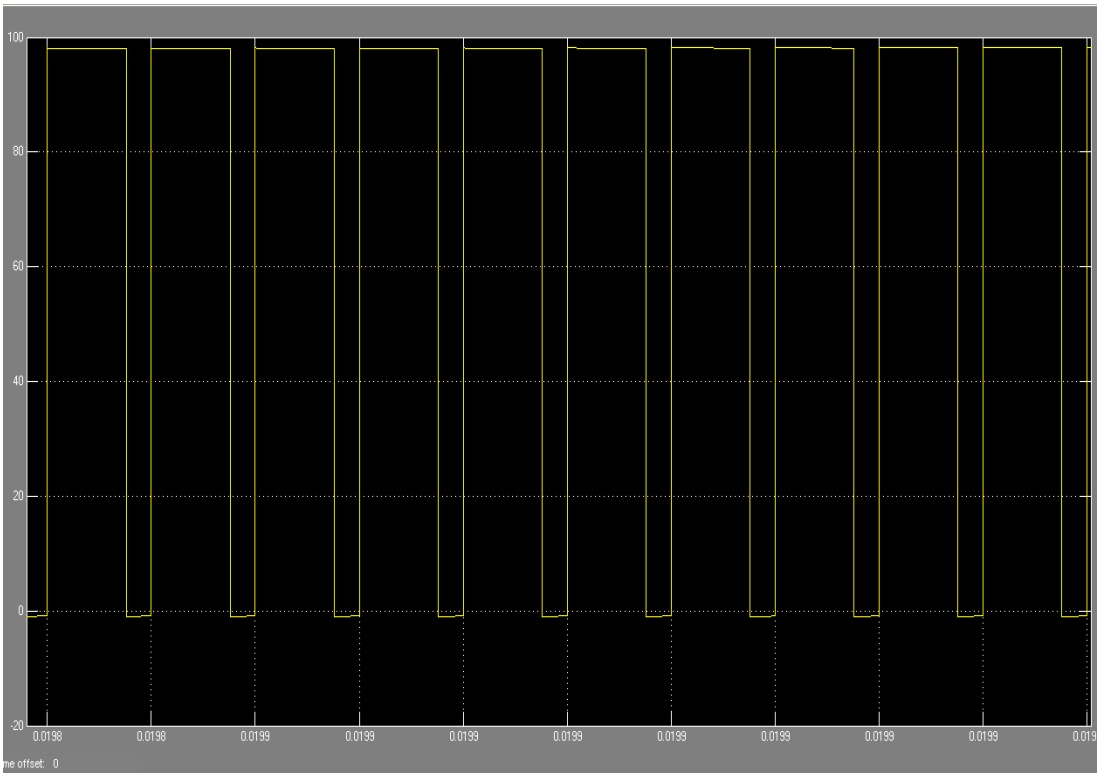

Figure 3.36: The Diode Voltage of Second Improved Topology

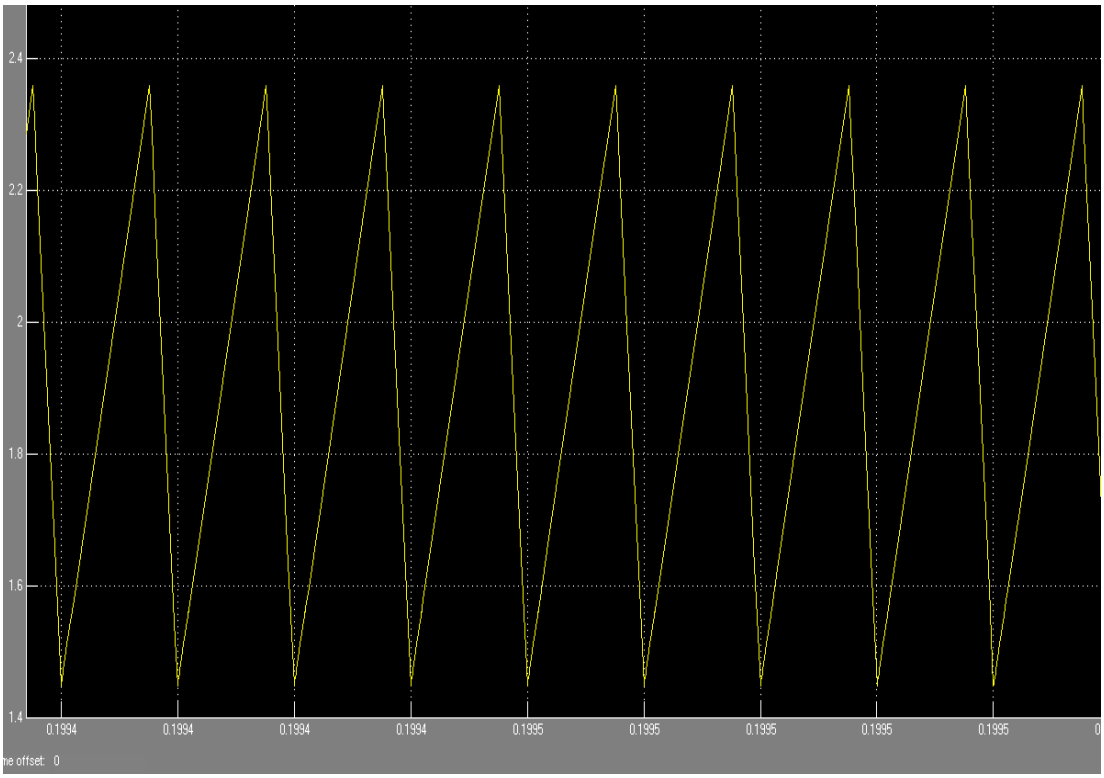

Figure 3.37: The L_1 Current of Second Improved Topology

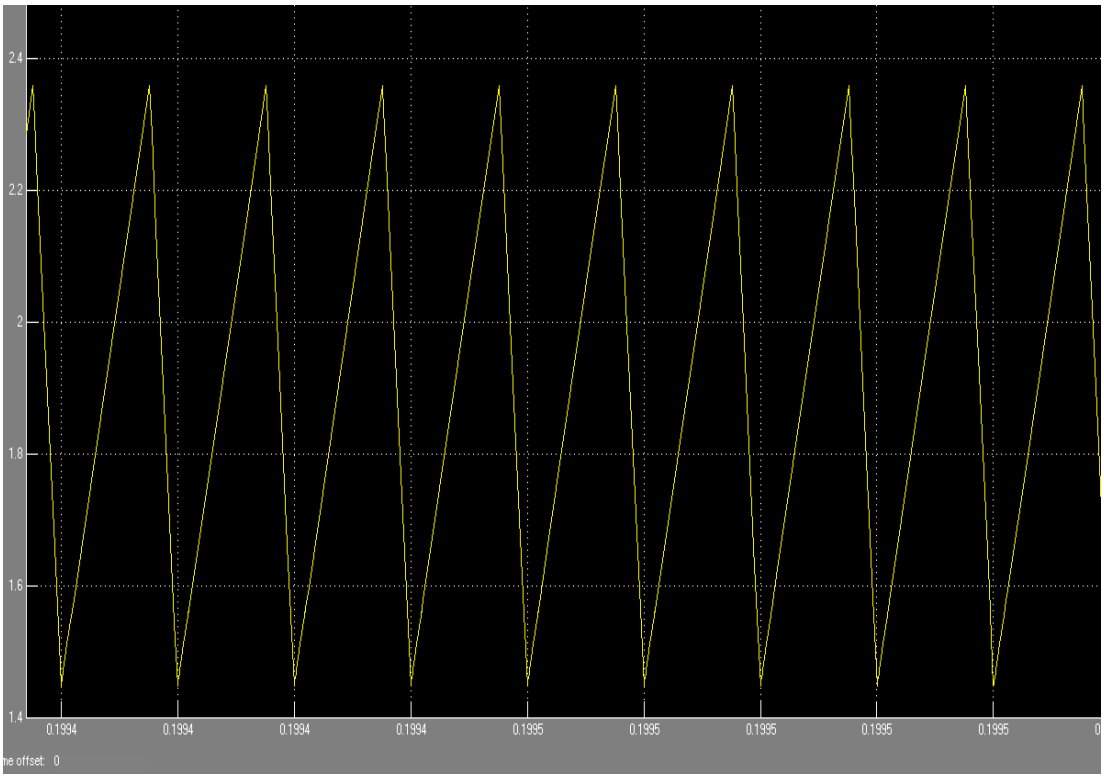

Figure 3.38: The L_2 Current of Second Improved Topology

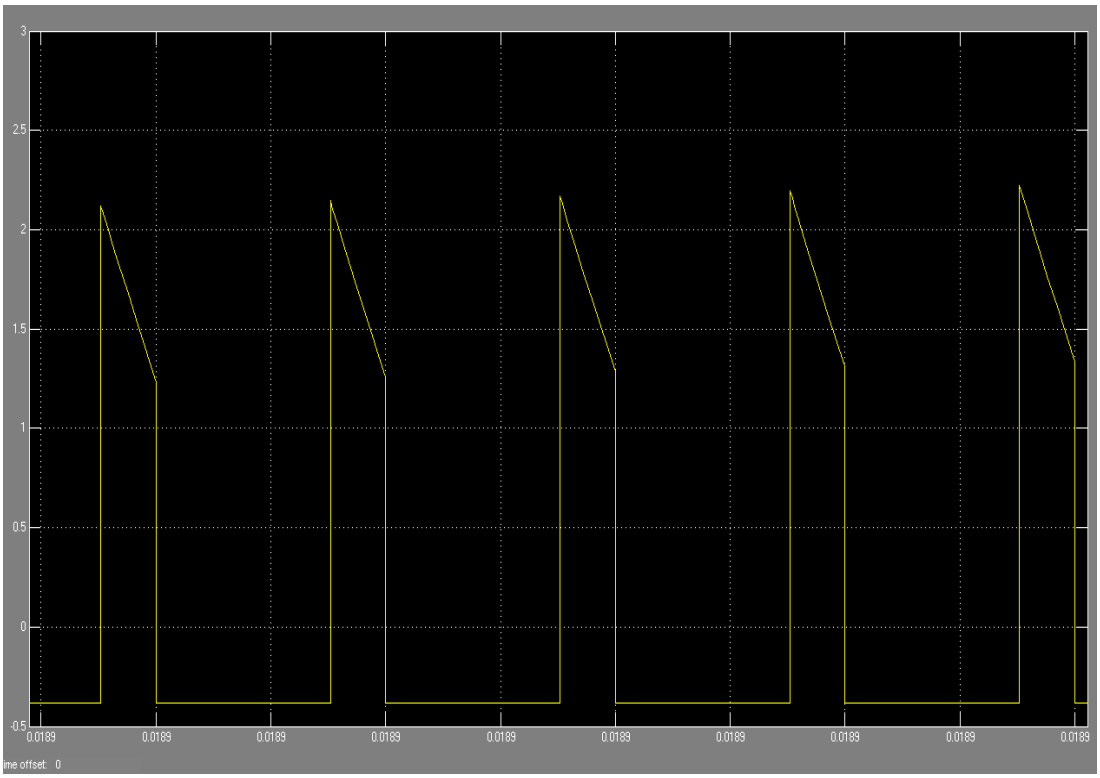

Figure 3.39: The Output Capacitor Current of Second Improved Topology

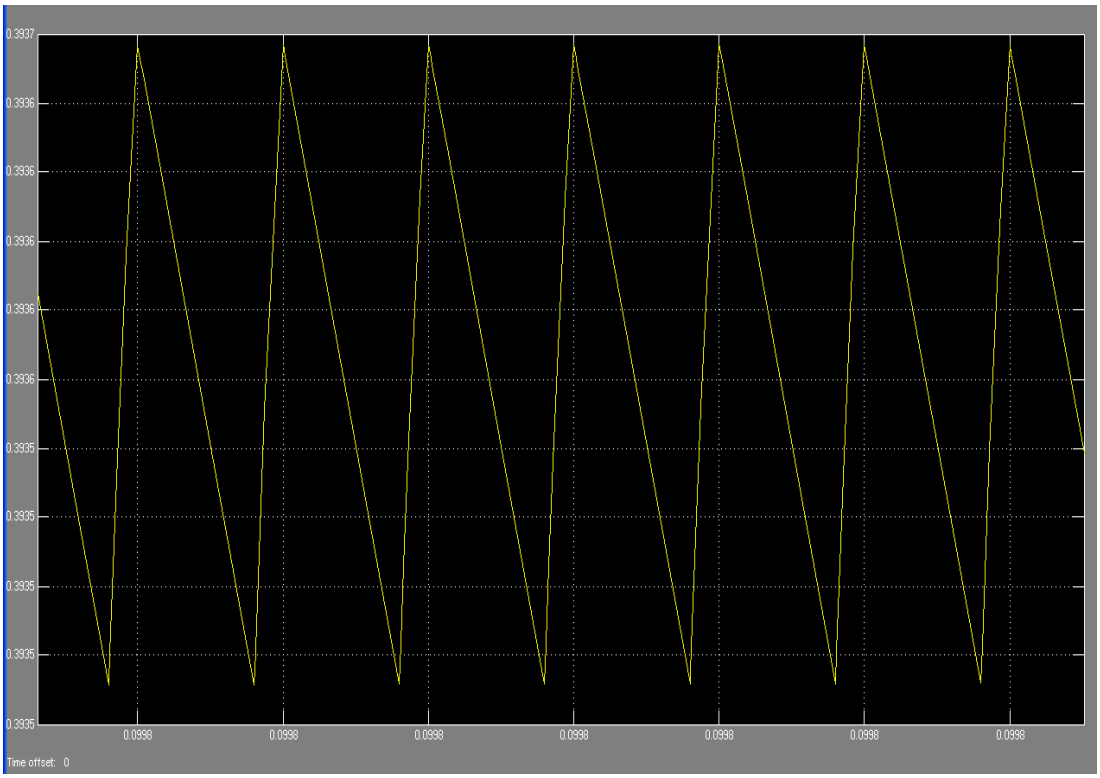

Figure 3.40: The Output Current of Basic Second Improved Topology

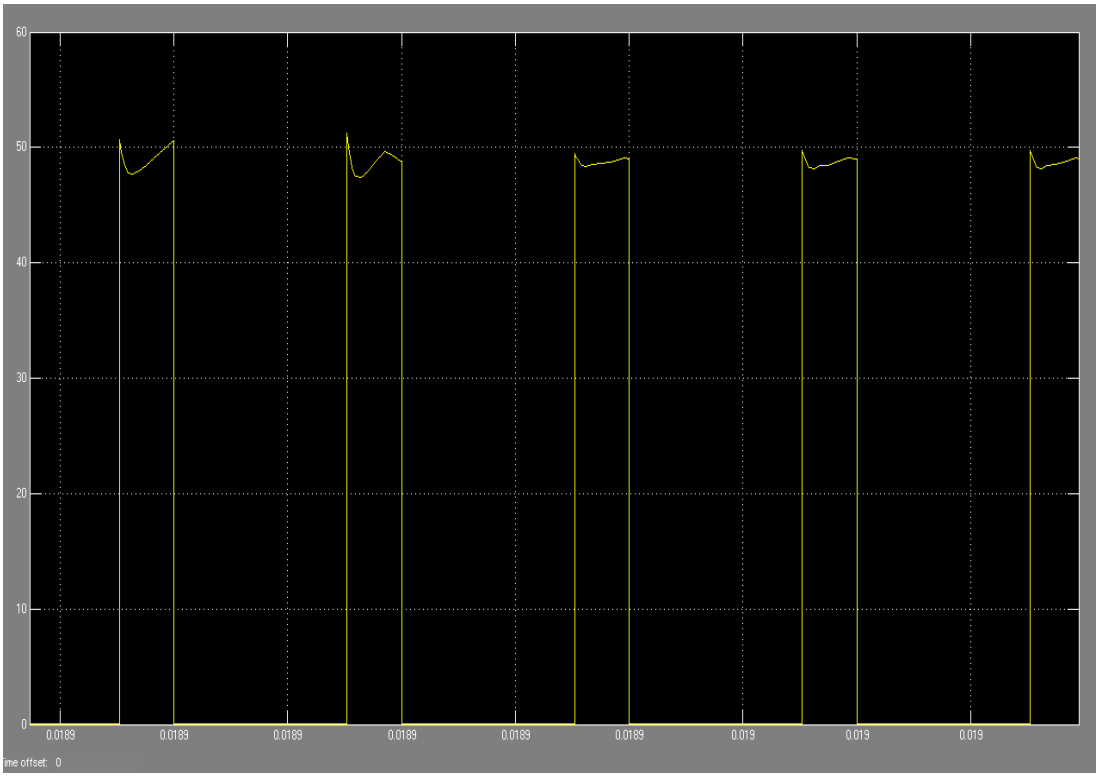

Figure 3.41: The Switch Voltage Stress V_{S1} of the Second Improved Topology

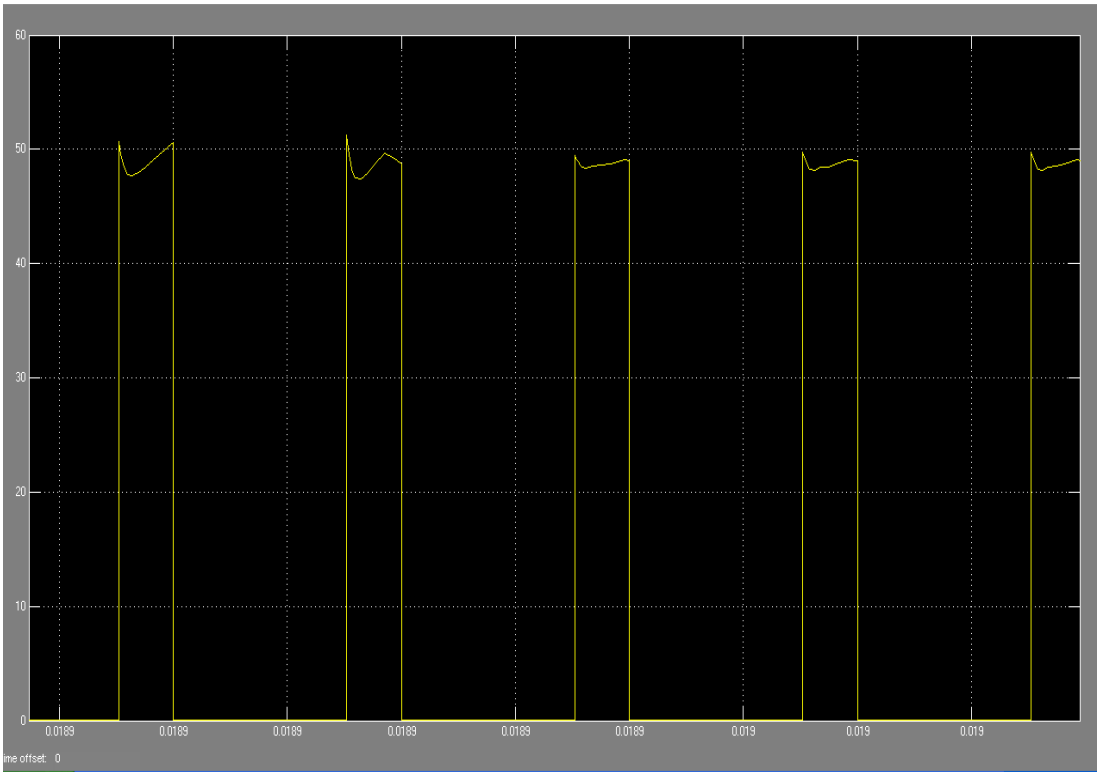

Figure 3.42: The Switch Voltage Stress V_{S2} of the Second Improved Topology

From Figures 3.37and 3.38, it is clearly shown the current value of the inductors $L_1$and L_2 are equal and it is approximately equal 2.5 ampere. Add to that the voltage across the output diode V_{DO} equal the output voltage V_O it is satisfy the equation (3.53).

To find power output in accordance with Figure 3.35and 3.40 the approximate value of V_o =98.2Vand the value of $I_o = 0.3937$A by substituting these values in (3.68).

$$P_o = V_o I_o \tag{3.68}$$

$$P_o = (98.155)(\ 0.3937) \approx 38.64\text{W}$$

By comparing the value of the power output in this topology with the first improved topology this topology raised the power output and the voltage gain. This mean the power losses and the voltage stress cross the two IGBT switches decrease and the value of the voltage stresses $V_{s1}$and V_{s2} are equal which are is clearly shown in Figure 3.41 and 3.42 .To obtain these values using (3.52).

$$V_{s1} = V_{s2} = \frac{(98.155)}{2} \approx 49.1\text{V} \quad (3.69)$$

3.7 The Third Improved Topology

This topology is similar to the first one except for adding two voltage lift circuits. Figure 3.43 shows this improved topology. In fact, this converter uses two inductors of the same inductance level, and the two switches being simultaneously . Similarly to the other converter circuits, the operation of such a converter is subdivided into two modes; the CCM and the DCM. Typical waveforms of these modes are depicted in Figure 3.44. The following subsections address the performance and steady state analysis of this converter.

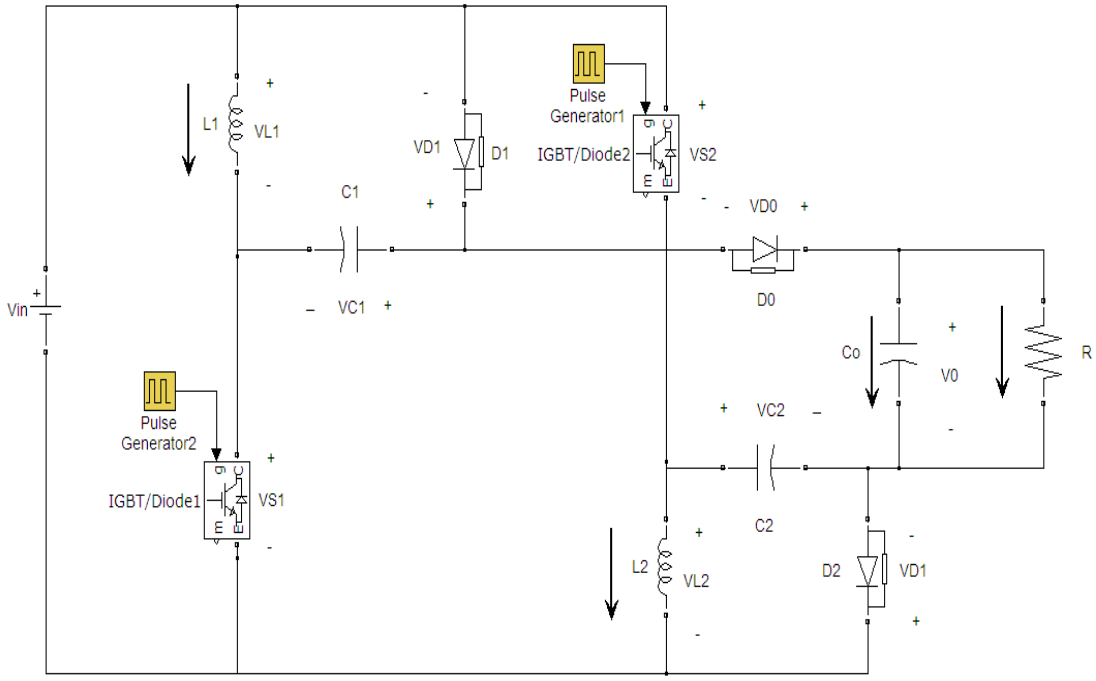

Figure 3.43: The Third Improved Topology

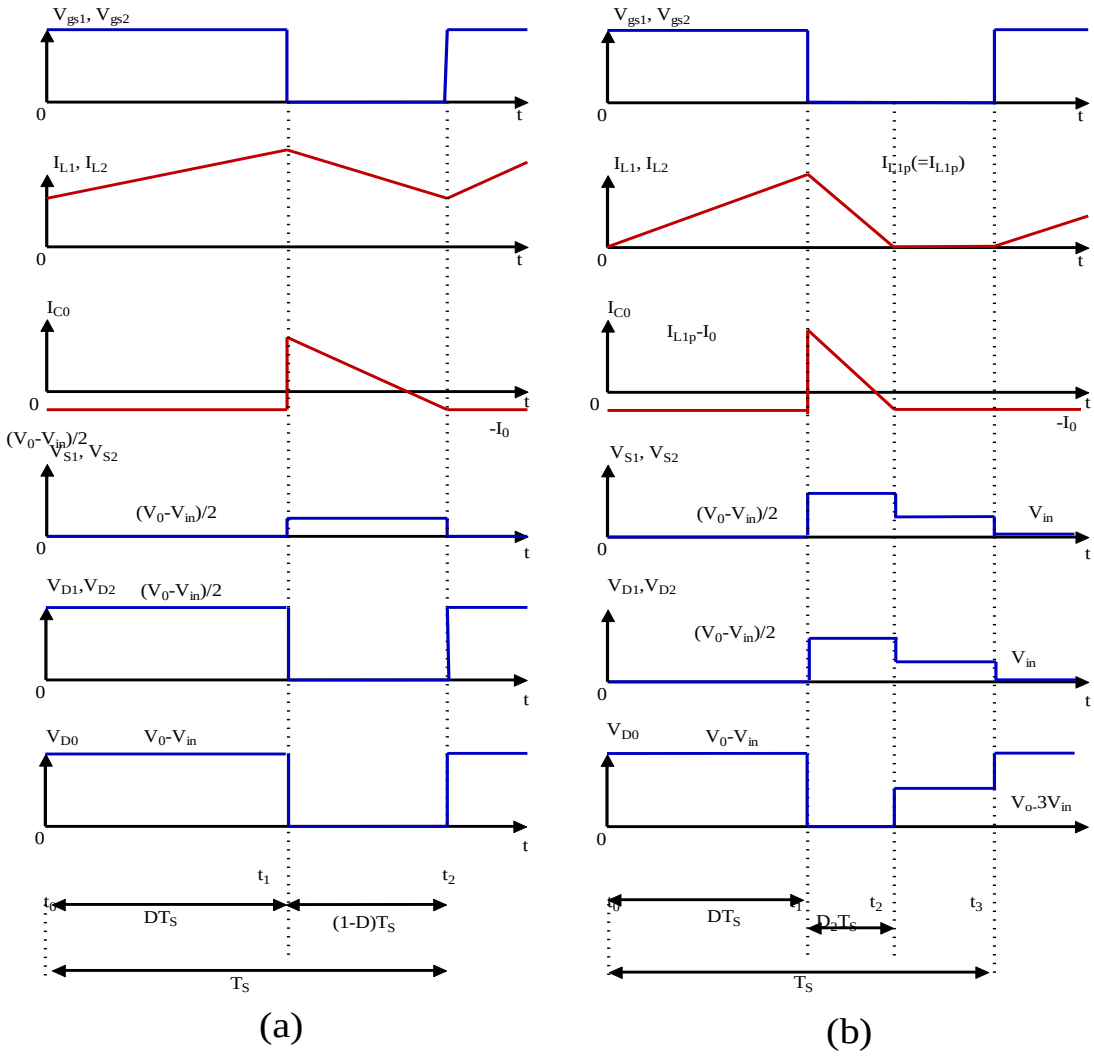

Figure 3.44: Typical Voltage and Current waveforms for the Third Topology

3.7.1 The Continuous Conduction Mode (CCM)

This mode of operation can be further divided into two stages:

Stage 1: This stage extends from t_0 to t_1 as sown in Figure 3.44-a. In this interval, switches S_1 and S_2 are both turned on, and the equivalent circuit of the converter will be as shown in Figure 3.45.During this stage, inductors L_1 and L_2 are charged in parallel from the DC source where as the capacitor C_o releases its energy to the load. Moreover, capacitors C_1 and C_2 are charged from the DC source.

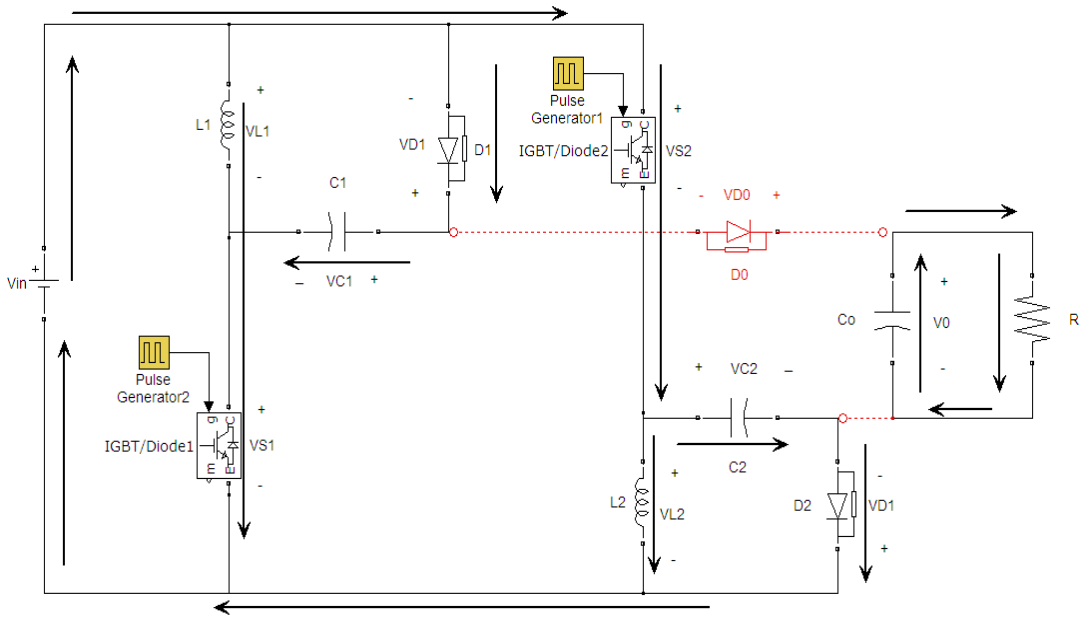

Figure 3.45: The Equivalent Circuit of CCM -stage 1 of the Third Topology

Considering the circuit of Figure 3.45 the voltages across L_1 , L_2 ,C_1 and C_2 are given by:

$$V_{L1} = V_{L2} = V_{in} = V_{L2} = V_{C2} \tag{3.70}$$

Stage 2: which extends from t_1 to t_2 appearing in Figure 3.44-a.During this time interval, S_1 and S_2 are switched off as shown in the equivalent circuit shown in Figure 3.46. Besides,L_1, L_2, C_1 and C_2 are connected in series to the DC source in order to transfer the stored energy to C_o and the load. So, the voltages across L_1 and L_2 are derived as:

$$V_{L1} = V_{L2} = \frac{V_{in}+V_{C1}+V_{C2}-V_o}{2} = \frac{3V_{in}-V_o}{2} \tag{3.71}$$

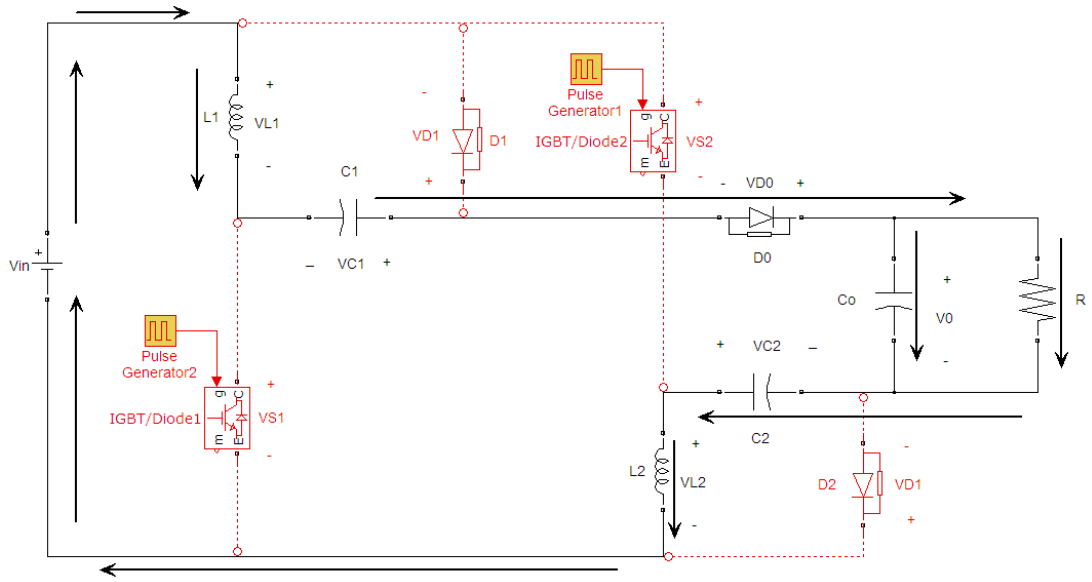

Figure 3.46: The Equivalent Circuit of CCM-stage 2 of the Third Topology

The fact that the two inductors are equal in values and have the same current implies the condition in (3.72). Doing the integration in (3.72), the voltage gain can be evaluated as in (3.73).

$$\int_0^{DT_S} V_{in}dt + \int_{DT_S}^{T_S} \frac{3V_{in}-V_0}{2} dt = 0 \tag{3.72}$$

The voltage gain is thus derived by rearranging (3.72), as follows:

$$\frac{V_o}{V_{in}} = \frac{3-D}{1-D} \tag{3.73}$$

Where, D is the duty cycle.

The voltage of the switches S_1 and S_2 is given by

$$\mathrm{V_{S1}} = \mathrm{V_{S2}} = \mathrm{V_{D1}} = \mathrm{V_{D2}} = \frac{V_o - V_{in}}{2} \tag{3.74}$$

Moreover, the diode voltage is

$$\mathrm{V_{Do}} = V_o - V_{in} \tag{3.75}$$

The voltage gain in (3.73) is plotted versus duty cycle (D) in Figure 3.47. Comparing the result obtained in this figure to that of the second proposed topology shown in Figure 3.31, the improvement in voltage gain with the second transformerless boost converter topology over that of the first one is notable.

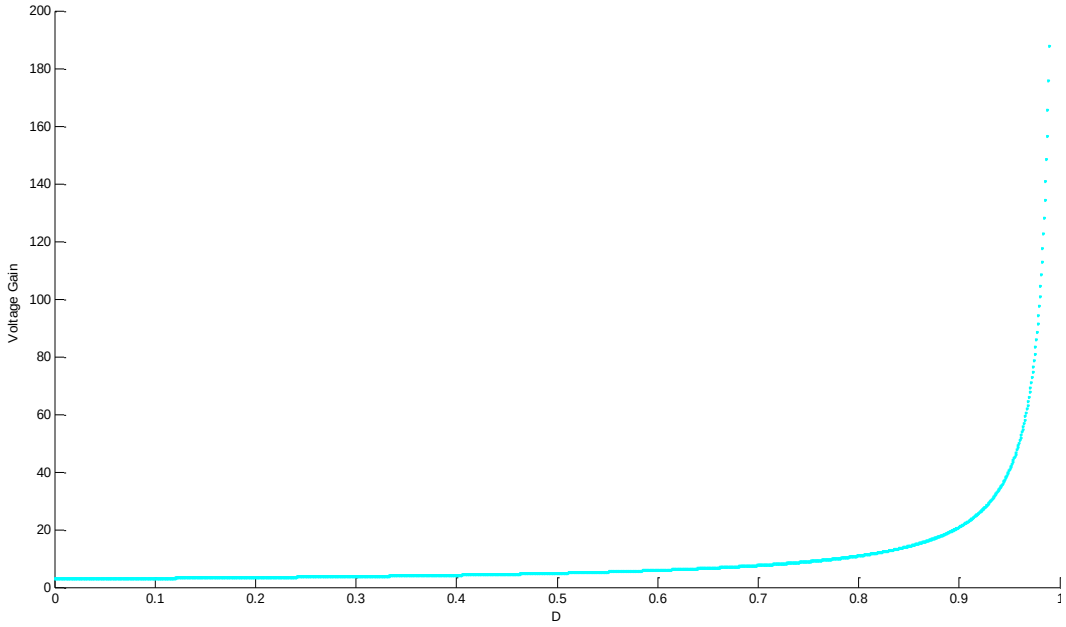

Figure 3.47: Voltage Gain versus Duty Cycle for the Third Topology in the CCM of the Third Topology

3.7.2 The Discontinuous Conduction Mode (DCM)

The DCM is also subdivided into three distinct stages:

Stage1: This takes place between t_0 and t_1 appearing in Figure 3.44-b. The status of the converter is the same as that of stage 1 in the CCM. During this stage the converter will have the equivalent circuit shown in Figure 3.45. The peak currents of inductors L_1 and L_2 can be found as ,

$$I_{L1p} = I_{L2p} = \frac{V_{in}}{L} DT_s \tag{3.76}$$

Stage 2: This extends from t_1 to t_2 appearing in Figure 3.44-b.In this time interval, the switches S_1 and S_2 are turned off, the inductors L_1 and L_2 and capacitors C_1 and C_2 are series connected with the DC source in order to transfer the stored energy to the capacitor C_o and the load, so the converter has the equivalent circuit shown in Figure 3.46.The inductor currents $\mathrm{i_{L1}}$ and $\mathrm{i_{L2}}$ start decreasing to zero at $t = t_2$. Another expression for $\mathrm{I_{L1p}}$and $\mathrm{I_{L2p}}$ is that of (3.77).

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_o - V_{in} - V_{C1-} V_{C1}}{2L} D_2 T_s$$

$$\mathrm{I_{L1p}} = \mathrm{I_{L2p}} = \frac{V_o - 3V_{in}}{2L} D_2 T_s \tag{3.77}$$

Stage 3: which occurs between t_2 and t_3 shown in Figure 3.44-b. During this time interval, S_1 and S_2 are still turned off, on the capacitor Co charges the R-load since the energy in L_1 and L_2 is zero. The equivalent circuit of the converter during this stage is explained in Figure 3.48.

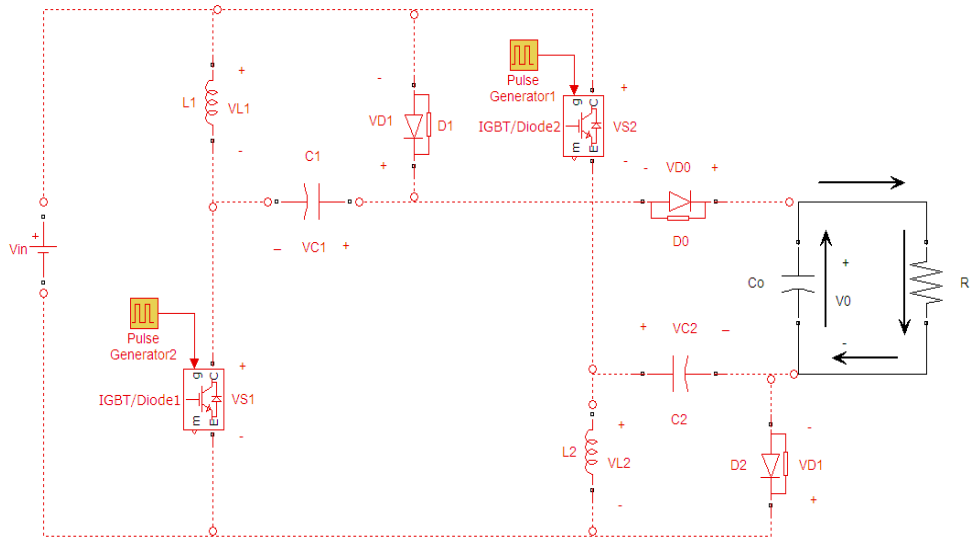

Figure 3.48: The Equivalent Circuit of DCM stage-3 of the Third Topology

Rearranging (3.76) and substituting (3.77), one can write:

$$\mathrm{D_2} = \frac{2\mathrm{DV_{in}}}{V_o - 3V_{in}} \tag{3.78}$$

Observing the waveform of I_{Co} in Figure 3.44-b, the average value of the capacitor output current during the whole period is found as follows:

$$I_{Co} = \frac{\frac{1}{2} D_2 T_S \mathrm{I_{L1p}} - \mathrm{I_O T_S}}{\mathrm{T_S}} = \frac{1}{2} D_2 \mathrm{I_{L1p}} - \mathrm{I_o} \tag{3.79}$$

Substituting (3.76) and (3.78) in (3.79), the result is:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - 3V_{in})} - \frac{V_o}{R} \tag{3.80}$$

Under the steady state condition, the capacitor output current equals zero, so:

$$I_{Co} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - 3V_{in})} - \frac{V_o}{R} = 0 \tag{3.81}$$

, or equivalently:

$$\frac{V_o}{R} = \frac{D^2 \mathrm{V_{in}}^2 T_S}{L(V_o - 3V_{in})} \tag{3.82}$$

Based on the aforementioned discussion, the voltage gain in this stage is given by:

$$\frac{V_o}{V_{in}} = \frac{3}{2} + \sqrt{\frac{9}{4} + \frac{D^2}{\tau_L}} \tag{3.83}$$

Based on (3.83), Figure 3.49 shows a plot of the voltage gain versus duty cycle in the discontinuous mode.

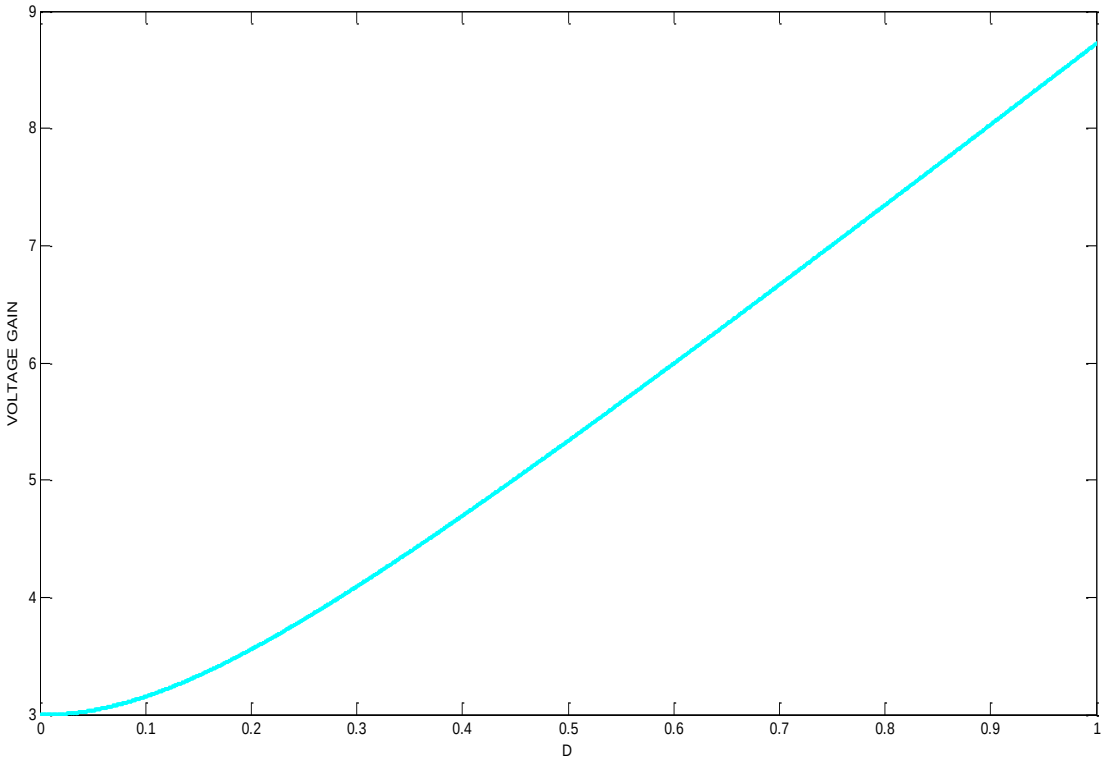

Figure 3.49: Voltage Gain versus Duty Cycle for the Second Topology in the DCM of the Third Topology

3.7.3 Boundary Operating Condition between CCM and DCM

Similarly to the other two converter topologies, this converter can also be operated in a boundary between the CCM and the DCM. In this situation, the voltage gain of the CCM equals that of the DCM, equating these gains given in (3.73) and (3.82), the boundary normalized inductor time constant τ_{LB} is given by:

$$\tau_{LB} = \frac{D(1-D)^2}{2(3-D)} \tag{3.84}$$

Figure 3.50 shows a plot of τ_{LB} versus D.

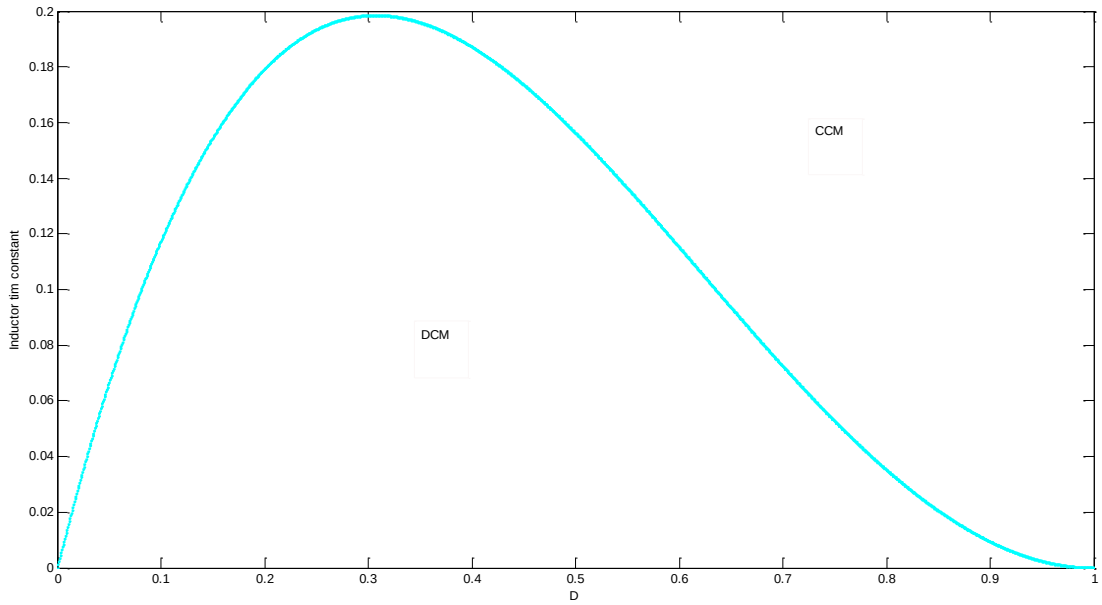

Figure 3.50: : Inductor Time Constant versus Duty Cycle for the First Topology in the Boundary Mode of the Third Topology

3.8 Calculations and Simulation Results of the Third Improved Topology

This section conveys simulation results of the third improved topology Figure 3.34 by using MATLAB Simulink. From reference [1],the value that are used are: L_1=$L_{2=}$100μH, P_o=40W,$V_{IN} = 12V$, $V_o = 100V$ and $C_1 = C_1 = 57\mu F$ *and* C_o=68μF , f_s=100KHz and, R_o=250 Ω.

To find the duty cycle D using (3.85).

$$\frac{V_o}{V_{in}} = \frac{3-D}{1-D} = \frac{100}{12} \tag{3.73}$$

So that,

D=0.72727= 72.727%

Figure 3.51 shows the output voltage V_o and Figure3.52 shows $V_{DO}$and also Figure 3.53and Figure3.54 shows the current during inductors I_{L1}, I_{L2} and Figure3.55 the current passed in the output capacitor I_{Co} and Figure 3.56 shows the output current

$I_o$finally Figures 3.57 and 3.58 delivered voltage switch stresses $V_{s1}$and V_{s2}, respectively.

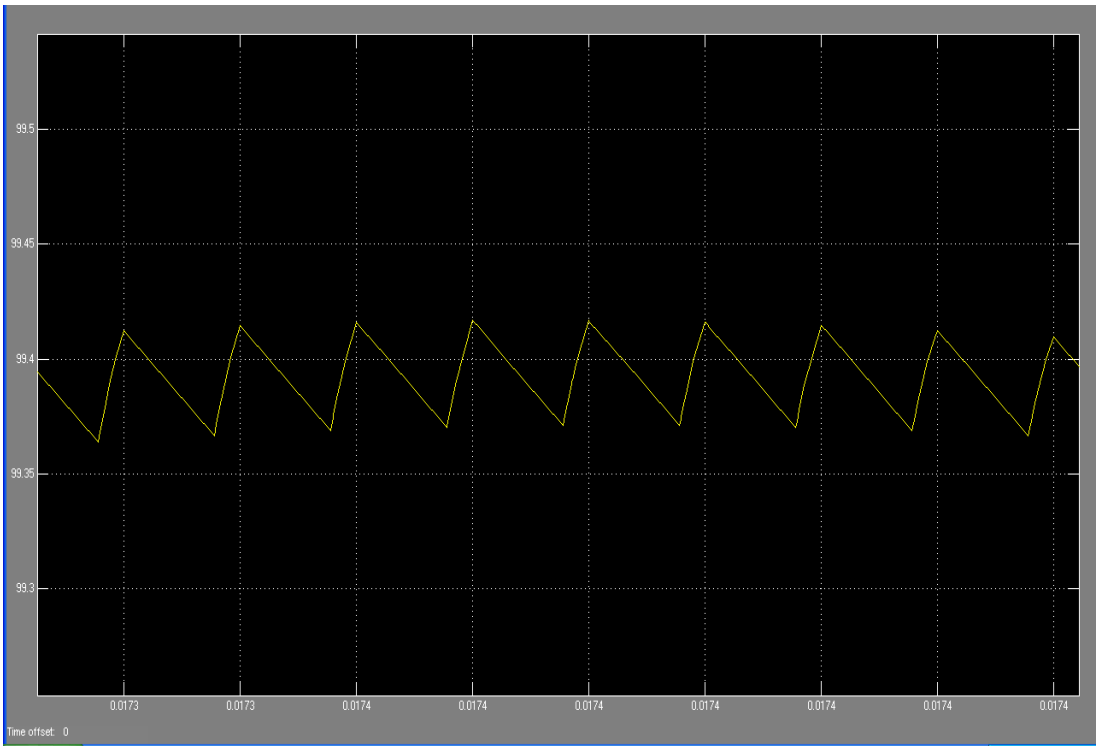

Figure 3.51: The Output Voltage of Third Improved Topology

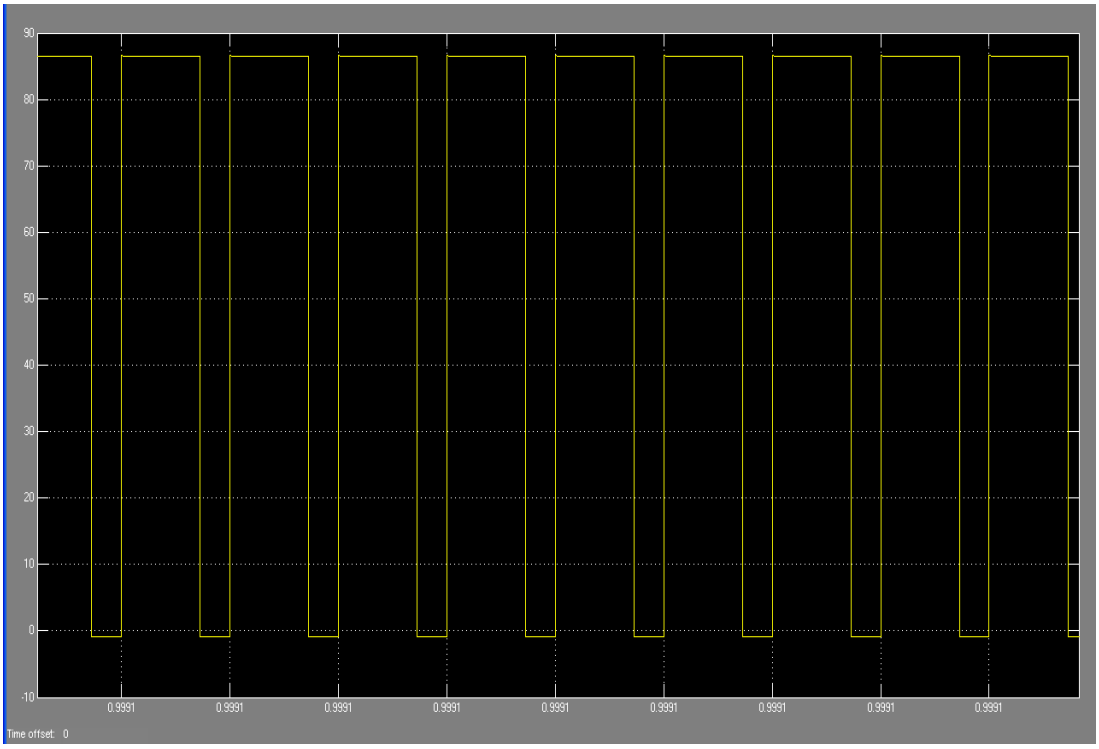

Figure 3.52: The Diode Voltage of Third Improved Topology

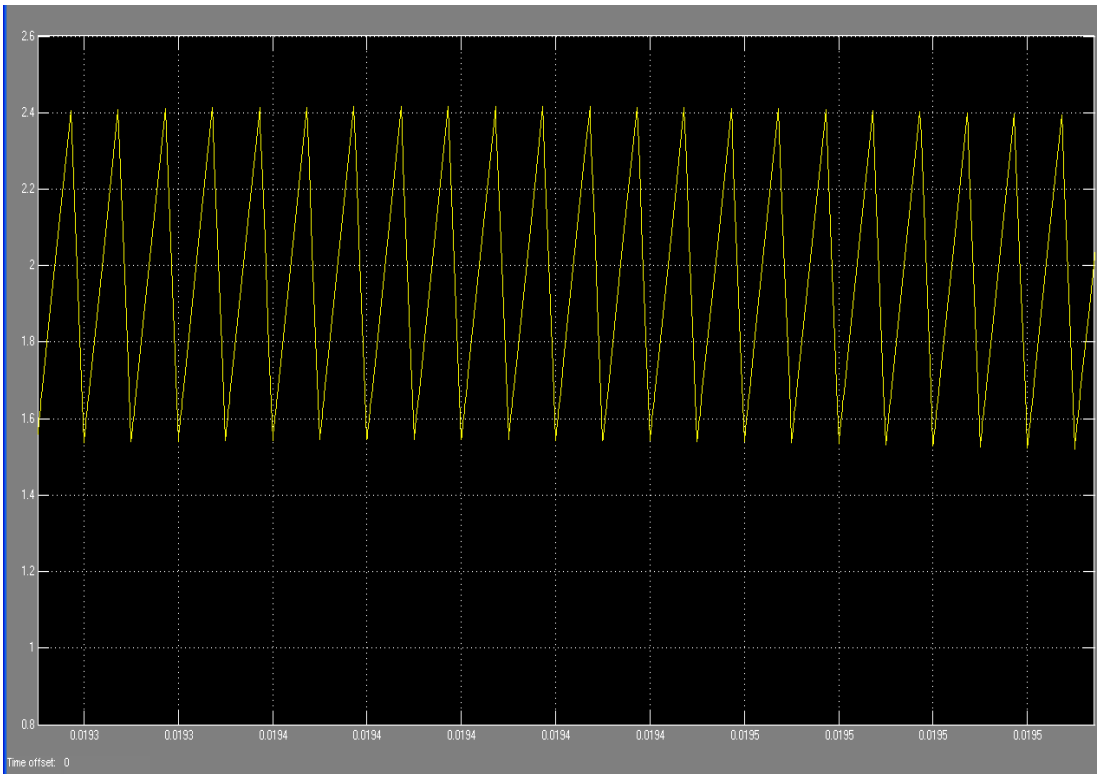

Figure 3.53: The L_1 Current of Third Improved Topology

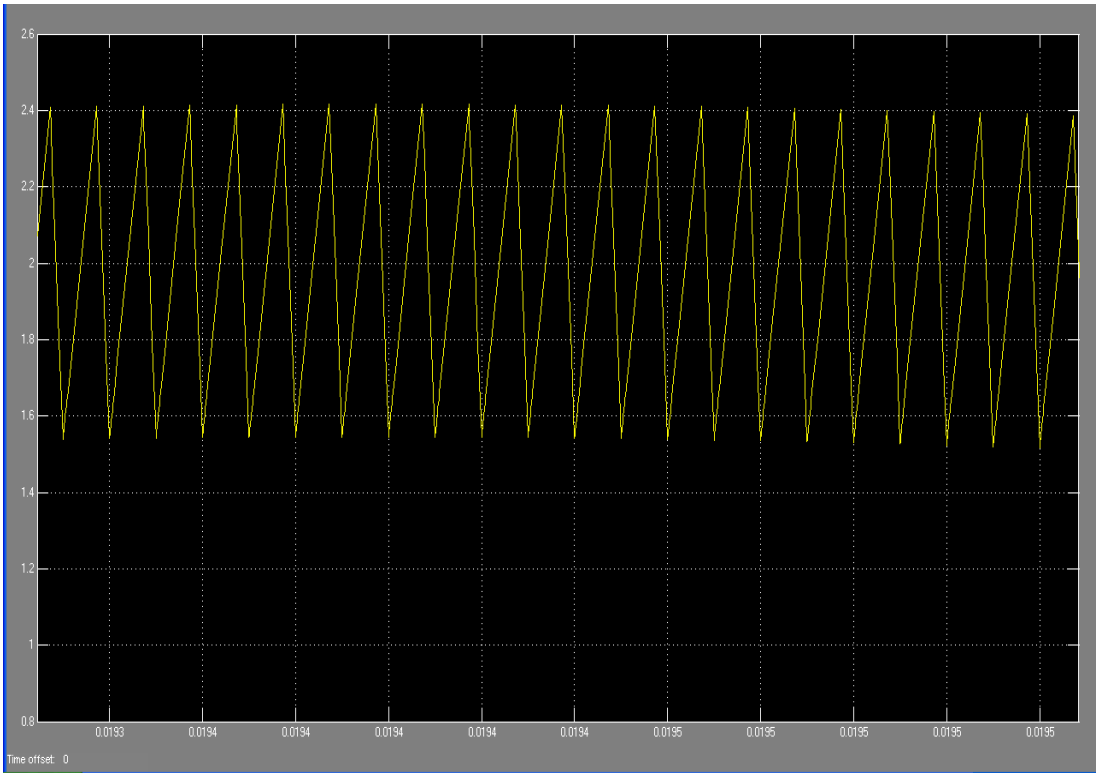

Figure 3.54: The L_2 Current of Third Improved Topology

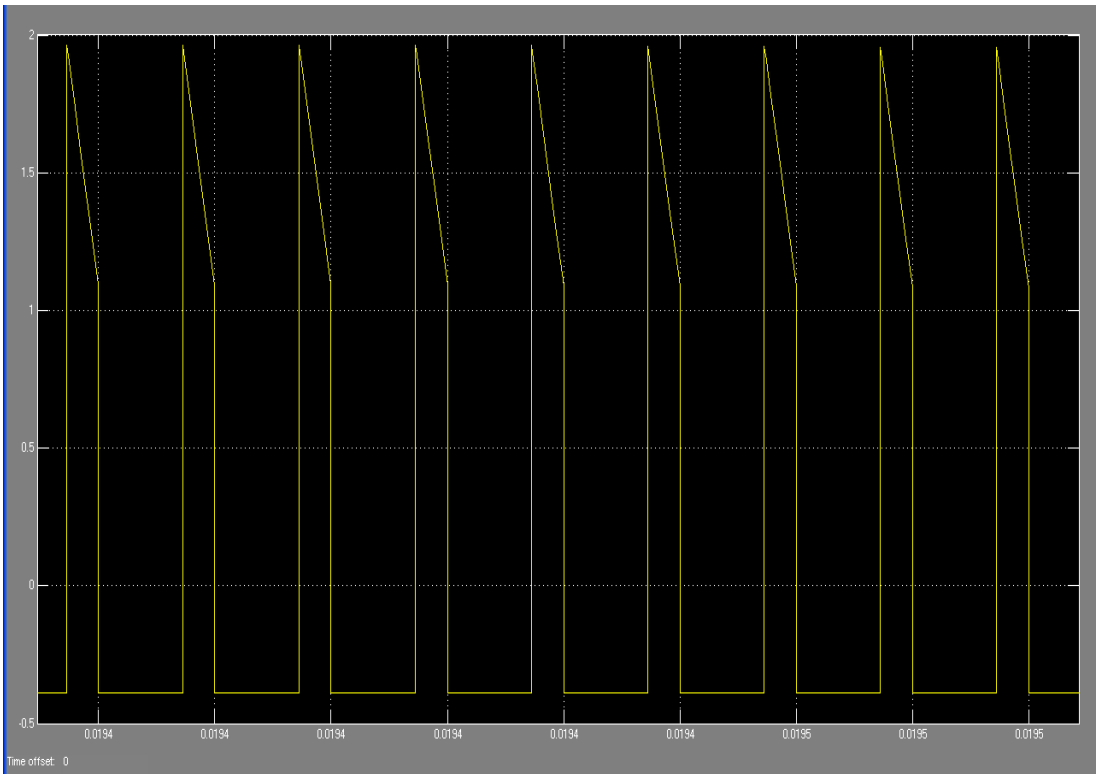

Figure 3.55: The Output Capacitor Current of Third Improved Topology

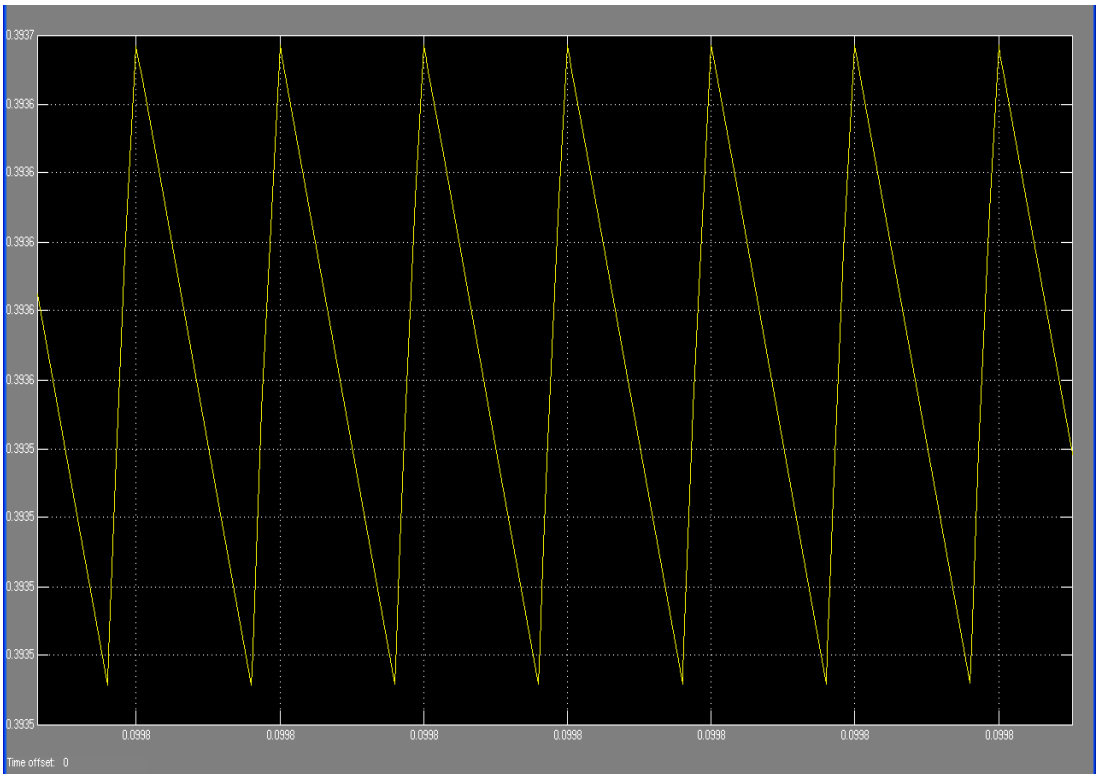

Figure 3.56: The Output Current of Basic Third Improved Topology

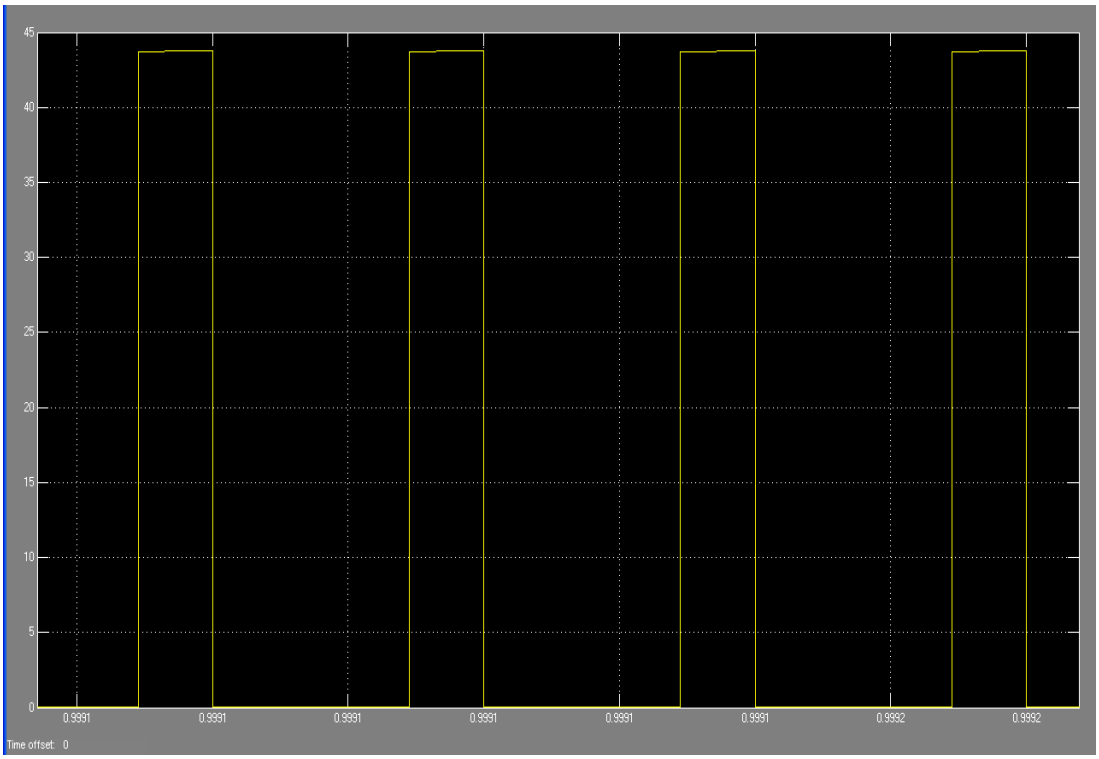

Figure 3.57: The Switch Voltage Stress V_{S1} of the Third Improved Topology

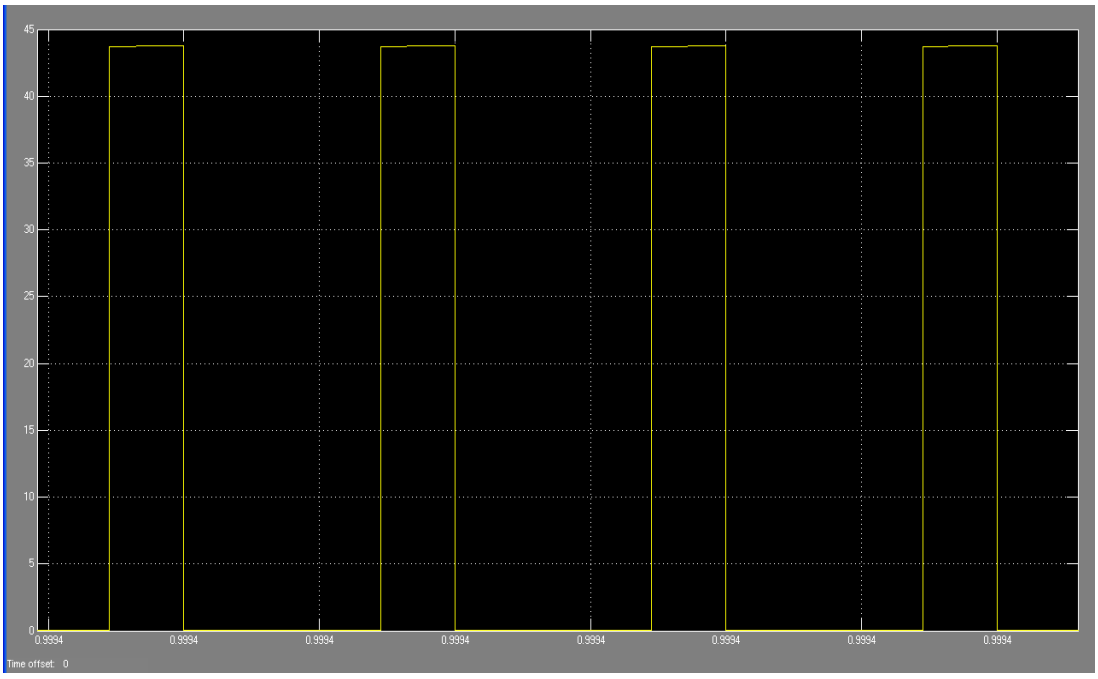

Figure 3.58: The Switch Voltage Stress V_{S2} of the Third Improved Topology

From Figures 3.53and 3.54 it is clearly shown the current value of the inductors $L_1$and L_2 are equal and it is approximately equal 2.4 ampere moreover from

Figure 3.51 and by using equation (3.75) the voltage across the output diode V_{Do} equal subtraction product the input voltage V_{in} from the output voltage V_o.

$$V_{Do} = V_o - V_{in}$$

$$V_{Do} = 99.41 - 12 \approx 87.41$$

This value viewed clearly in Figure 3.52.

To find power output in accordance with Figures 3.51and3.56 the approximate value of V_o ≈99.41Vand the value of $I_o \approx 0.3937$A by substuited these value in this formula (3.85).

$$P_o = V_o I_o \tag{3.85}$$

$$P_o = (99.41)(\ 0.3937) \approx 39.138\text{W}$$

By comparing the value of the power output in this topology with the second improved topology this topology raised the power output and the voltage gain its mean the power losses and the voltage stress cross two IGBTswitchs decrease and the value of the voltage stress V_{s1} and V_{s2} are equal it is clearly shown in Figures 3.57 and 3.58 to obtaining these values using formula (3.74)

$$V_{s1} = V_{s2} = \frac{V_o - V_{in}}{2}$$

$$V_{s1} = V_{s2} = \frac{(99.41 - 12)}{2} \approx 43.705\text{V}$$

3.9 Comparison between the Three Proposed Topologies and the simple Boost Topology

Table 3.1 summarises comparison between the simple and the three improved boost converter topologies in terms of voltage gain and active switch voltage stress. Considering the table values, it is clear that the three improved topologies have a lower switch voltage stress than the simple one. This add-value gives the possibility of using switches of lower voltage ratings and lower on-state resistance. In terms of

voltage gain, Figure 3.59 shows the voltage gains of the simple boost converter and the three improved topologies which have a higher value of voltage gain as seen in the figure.

	Voltage Gain	Voltage Stress
Simple Converter	$\frac{1}{1-D}$	V_o
The First Improved Topology	$\frac{1+D}{1-D}$	$\frac{V_o + V_{in}}{2}$
The Second Improved Topology	$\frac{2}{1-D}$	$\frac{V_o}{2}$
The Third Improved Topology	$\frac{3-D}{1-D}$	$\frac{V_o - V_{in}}{2}$

Table 1: Comparison of the Simple and the Three Improved Topologies

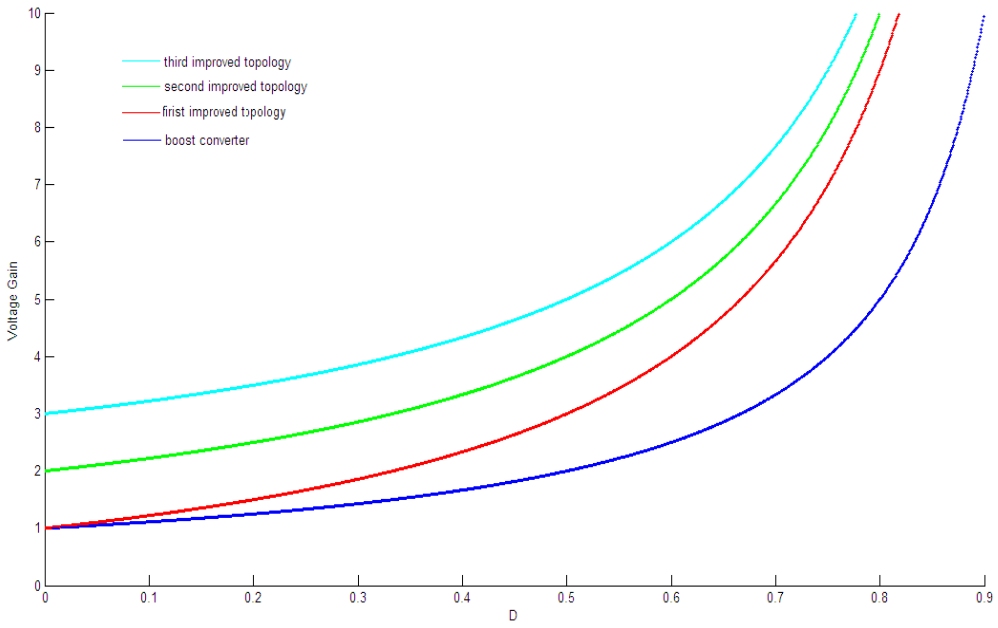

Figure 3.59: Voltage Gain Comparison of the Simple and the Three Improved Topologies

3.10 Efficiency Comparison between the Three Proposed Topologies and the Simple Boost Topology

The efficiency of an entity (a device, component, or system) in electronics and electrical engineering is defined as useful power output divided by the total electrical power consumed. Table 3.2, 3.3, 3.4 and 3.5 shows the power efficiency calculation of simple boost topology and three proposed topologies in terms of power efficiency and duty cycle, figure3.60 summarises comparison between the simple and the three improved boost converter topologies in terms of power efficiency as a function of duty cycle. It is clear that the three improved topologies have high power efficiency than the simple one as seen in the figure.

Duty Cycle	V_{IN}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency (%)
0.1	12	0.24	13.23	0.053	2.88	0.702	20.2
0.2	12	0.31	14.21	0.057	3.72	0.81	21.89
0.3	12	0..395	16.54	0.064	4.74	1.058	22.3
0.4	12	0.49	18.65	0.072	5.89	1.343	22.8
0.5	12	0.64	23.41	0.099	7.68	2.317	30.2
0.6	12	0.76	29.11	0.116	9.12	3.376	37.17
0.7	12	0.95	39.33	0.157	11.4	6.17	54.1
0.8	12	1.43	58.54	0.234	17.16	13.698	79.83
0.9	12	3.77	97.44	0.389	45.24	37.89	83.75

Table 2: Efficiency Calculation of the Simple Boost converter

Duty Cycle	V_{IN}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency (%)
0.1	12	0.22	14.12	0.056	2.64	0.791	29.95
0.2	12	0.31	17.66	0.065	3.72	1.1479	30.85
0.3	12	0.38	22.12	0.07	4.56	1.548	33.95
0.4	12	0.61	27.77	0.09	7.32	2.499	34.1
0.5	12	1.15	35.56	0.14	13.8	4.622	36.1
0.6	12	1.32	47.34	0.17	15.84	8.05	50.08
0.7	12	1.76	66.98	0.27	21.12	18.08	85.62
0.8	12	3.5	98.45	0.39	42	38.395	91.5
0.9	12	17.9	224	0.89	205.32	199.36	92

Table 3: Efficiency Calculation of the First Improved Topology

Duty Cycle	V_{IN}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency (%)
0.1	12	0.568	25.98	.096	6.82	2.494	36.56
0.2	12	0.731	29.61	0.114	8.78	3.375	38.4
0.3	12	0.9	33.87	0.133	10.8	4.505	41.6
0.4	12	1.108	39.76	0.156	13.3	6.202	46.3
0.5	12	1.425	47.86	0.193	17.1	9.23	53.7
0.6	12	1.84	58.43	0.248	22.1	14.48	65.3
0.7	12	2.458	79.3	0.33	29.5	26.169	88.7
0.8	12	4.24	110.76	0.425	50.9	47.1	92.5
0.9	12	19.93	238.97	0.943	239.22	225.35	94.2

Table 4: Efficiency Calculation of the Second Improved Topology

Duty Cycle	V_{IN}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency (%)
0.1	12	1.21	37.89	0.155	14.5	5.87	40.54
0.2	12	1.36	41.2	0.172	16.35	7.09	43.38
0.3	12	1.38	45.33	0.18	16.5	8.16	48.98
0.4	12	1.39	50.9	0.21	16.66	10.69	64.8
0.5	12	1.6	58.93	0.24	19.23	14.14	73.5
0.6	12	1.95	70.43	0.29	23.4	20.42	87.9
0.7	12	3.04	91.32	0.37	36.5	33.79	92.7
0.8	12	6.45	130.9	0.55	77.4	71.99	93.8
0.9	12	21.1	251.33	0.99	255.7	248.8	97.3

Table5: Efficiency Calculation of the Third Improved Topology

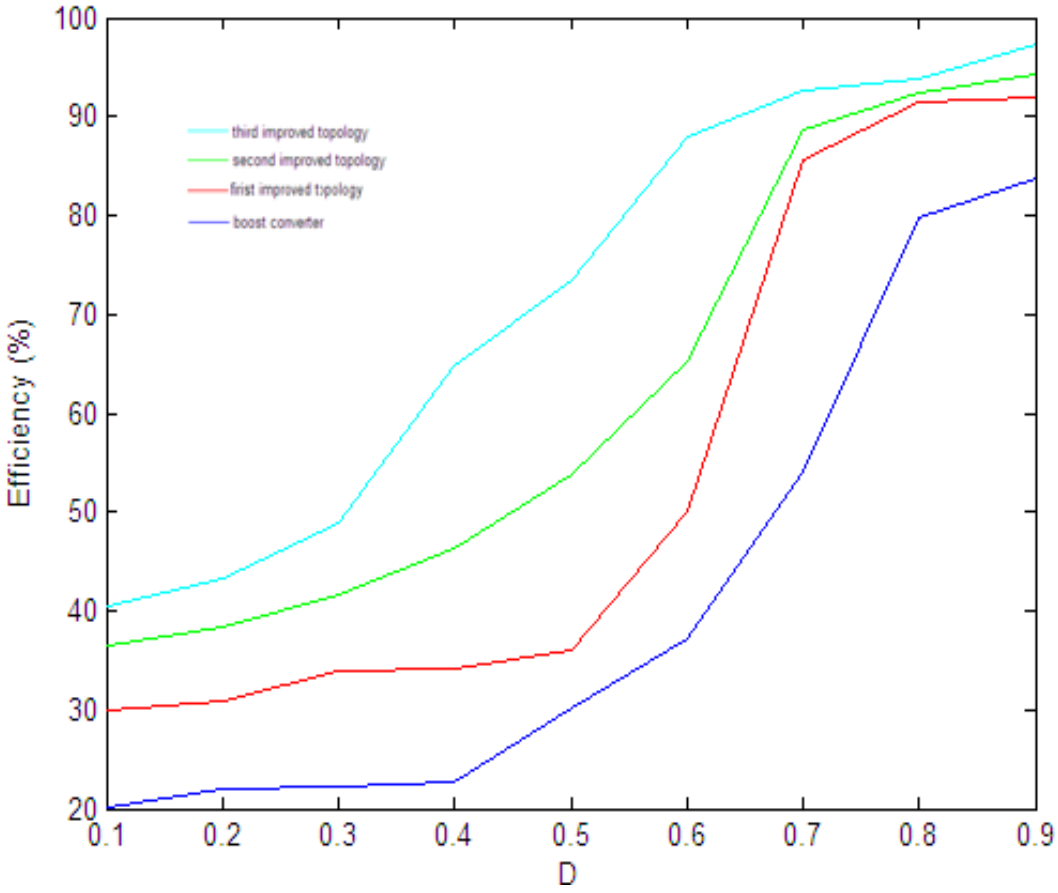

Figure 3.60: Efficiency Comparison of the Simple and the Three Improved Topologies

Chapter 4

EXPERIMENTAL RESULTS

4.1 Introduction

This chapter describes the practical implementation results of two converter circuits; the simple converter Figure 2.1and the basic converter topology Figure 3.1. These two circuits were practically implemented and certain measurements were made including, the input and output voltages and the switch voltage stress. These results are givven in the following sections.

4.2 Simple Converter Implementation

The simple converter shown in Figure 2.2 was practically implemented; a picture of the implemented circuit is shown Figure 4.1. The following components were used:

- The IRFP450 MOSFET
- Capacitor Co of 150 μF
- An inductor of 50μH
- A 6A05-6A10 diode
- A 400 Ω resistor

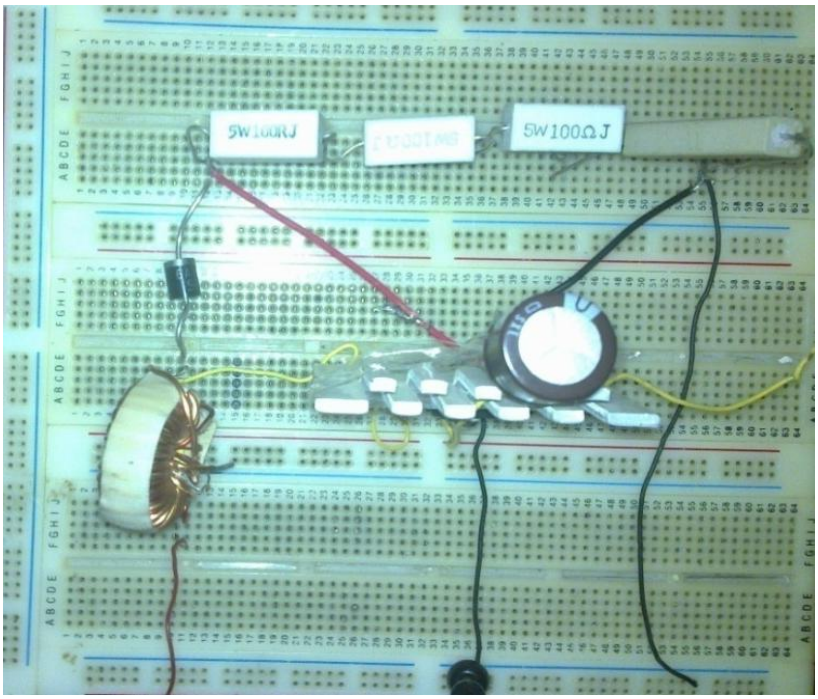

Figure 4.1: The implemented circuit of the Simple Boost Converter

A switching frequency of 6.9 kHz with square pulse of 50% duty cycle and 20 volt for operating the gate was used. Then, the input voltage, the output voltage and the MOSFET voltage stress and the waveforms were observed, captured and shown in Figures 4.2, 4.3, 4.4, and 4.5, respectively.

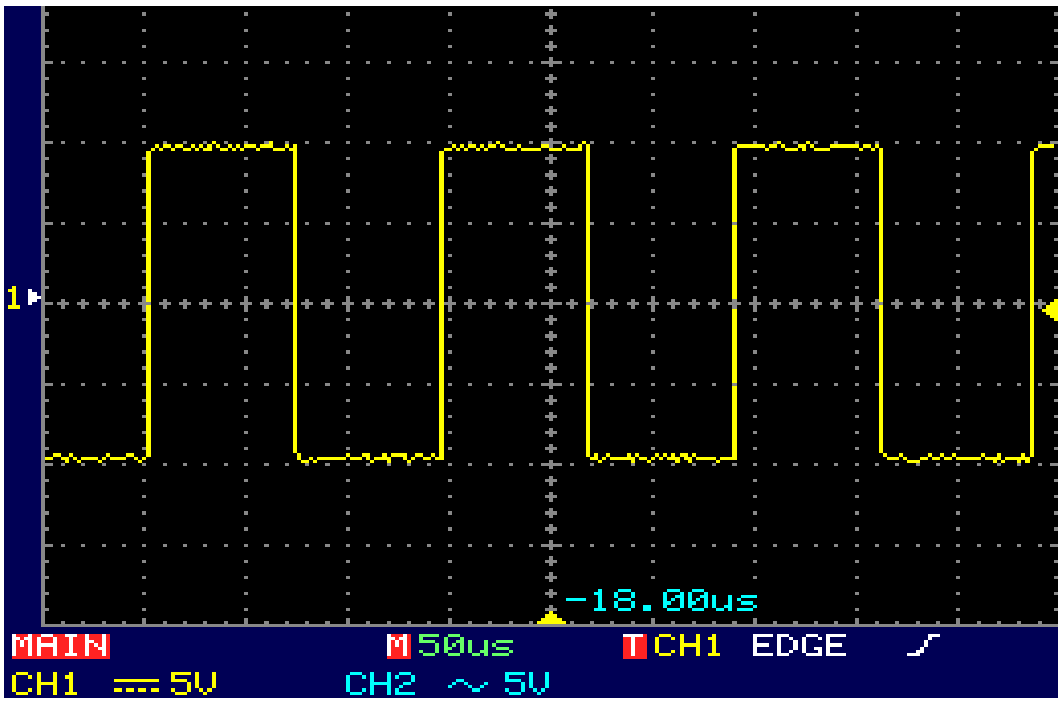

Figure 4.2: The Input pulse of MOSFET gate

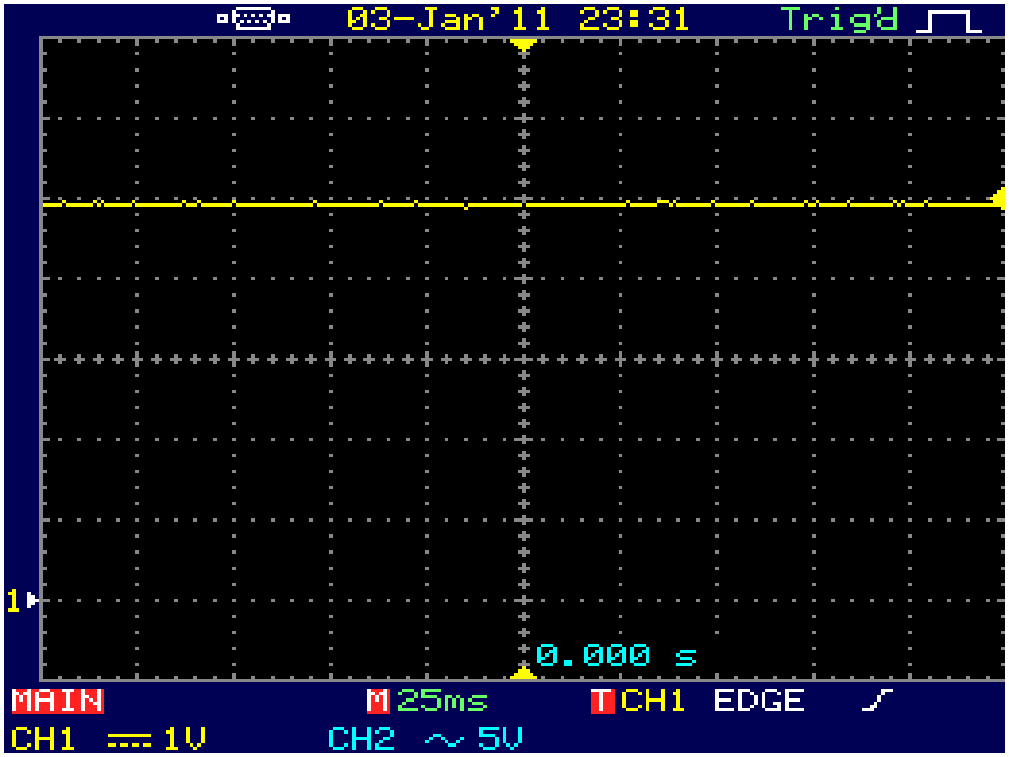

Figure 4.3: The Input Voltage of the Simple Boost Converter

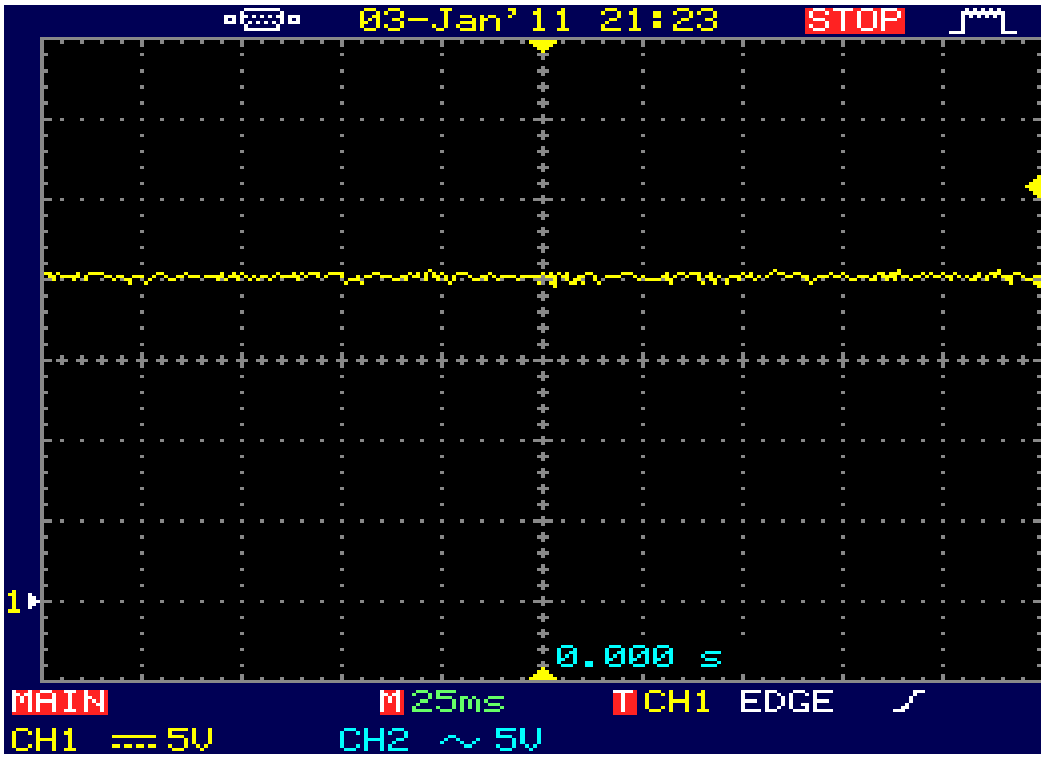

Figure 4.4: The Output Voltage of the Basic Boost Converter

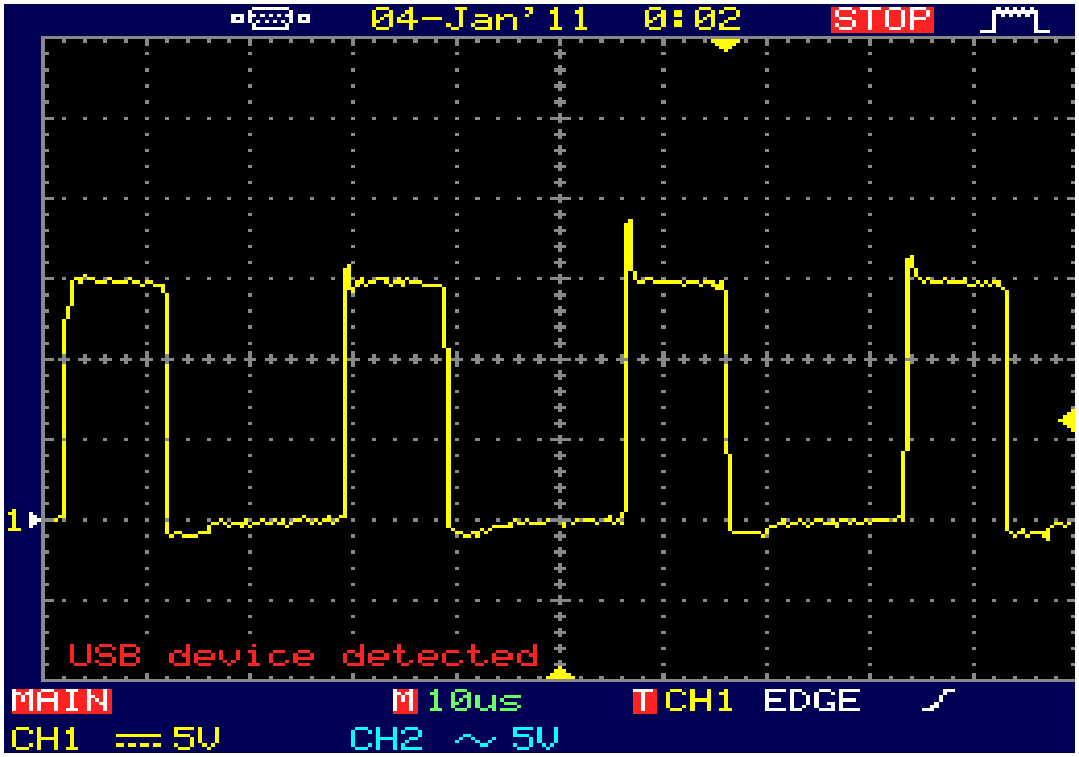

Figure 4.5: The MOSFET Voltage Stress of the Simple Boost Converter

4.3 Basic Converter Implementation

The basic converter topology is shown in Figure 3.1. The Figure 4.6 shows a picture of the implementation circuit which was practically implemented using the following components:

- The IRFP450 MOSFET
- Capacitor Co of 150 µF
- Two inductors of 50µH
- Four 6A05-6A10 diodes
- A 400 Ω resistor

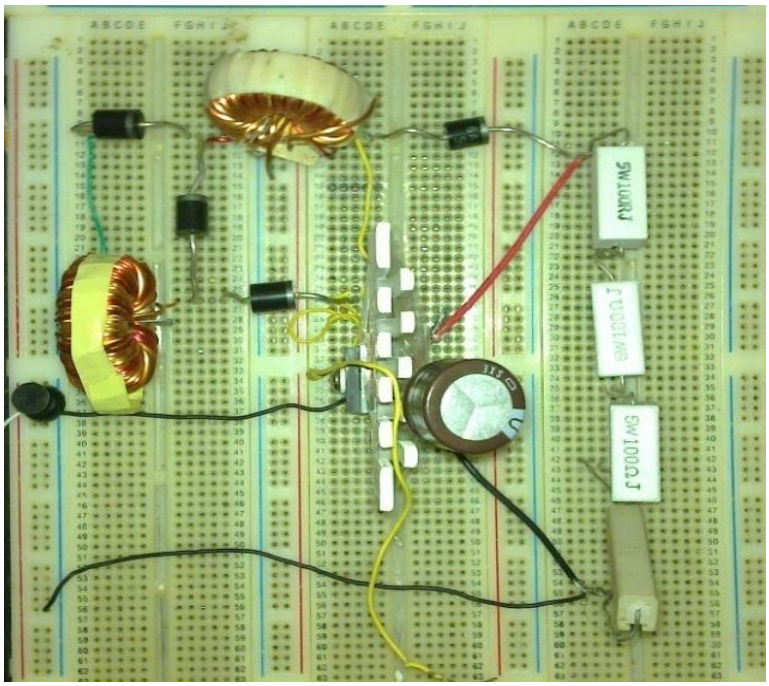

Figure 4.6: The implemented circuit of the Basic Boost Converter

A switching frequency of 6.9 kHz with squire pulse of 50% duty cycle and 20 volt for operating the gate was used clearly shown in figure 2.2. After that, the input voltage, the output voltage, and the MOSFET voltage stress were explored by an oscilloscope. These waveforms were snapped from the oscilloscope and are shown in Figure, 4.7, 4.8 and 4.9, respectively.

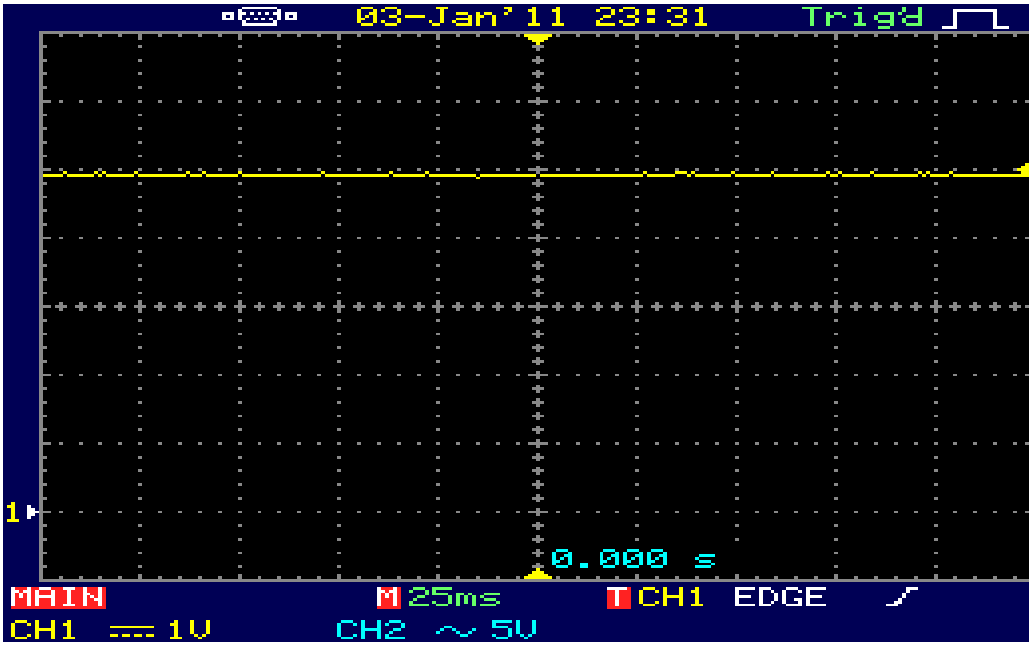

Figure 4.7: The Input Voltage of the Basic Boost Converter

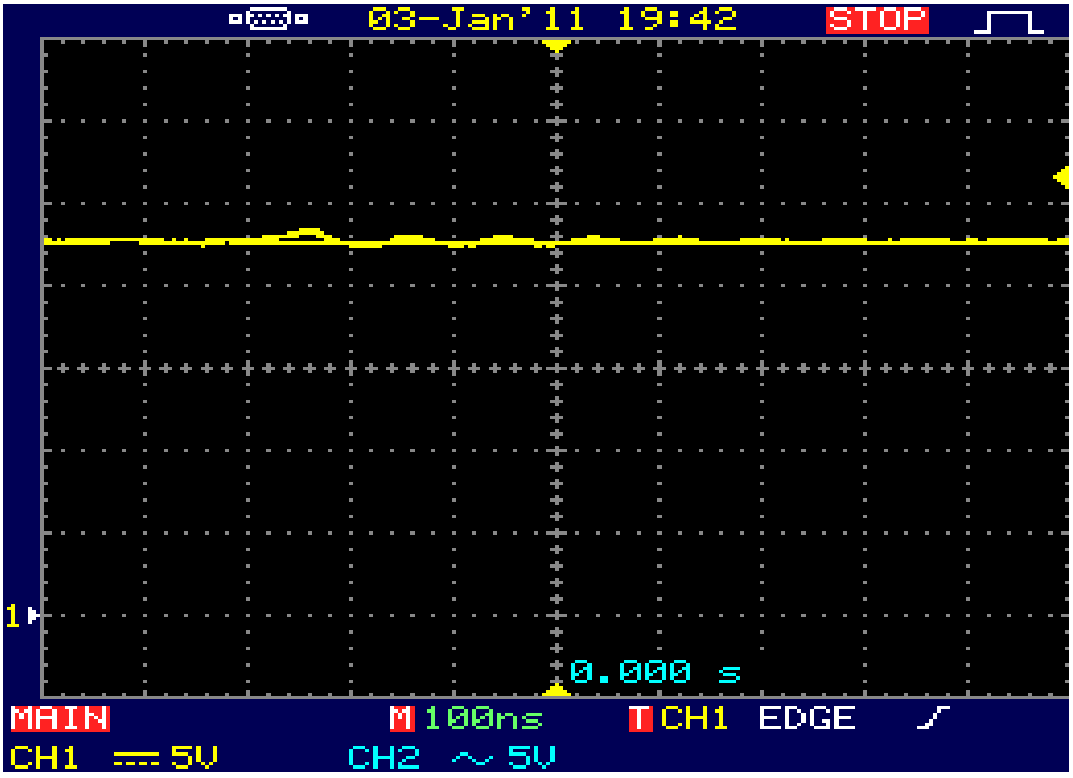

Figure 4.8: The Output Voltage of the Basic Boost Converter

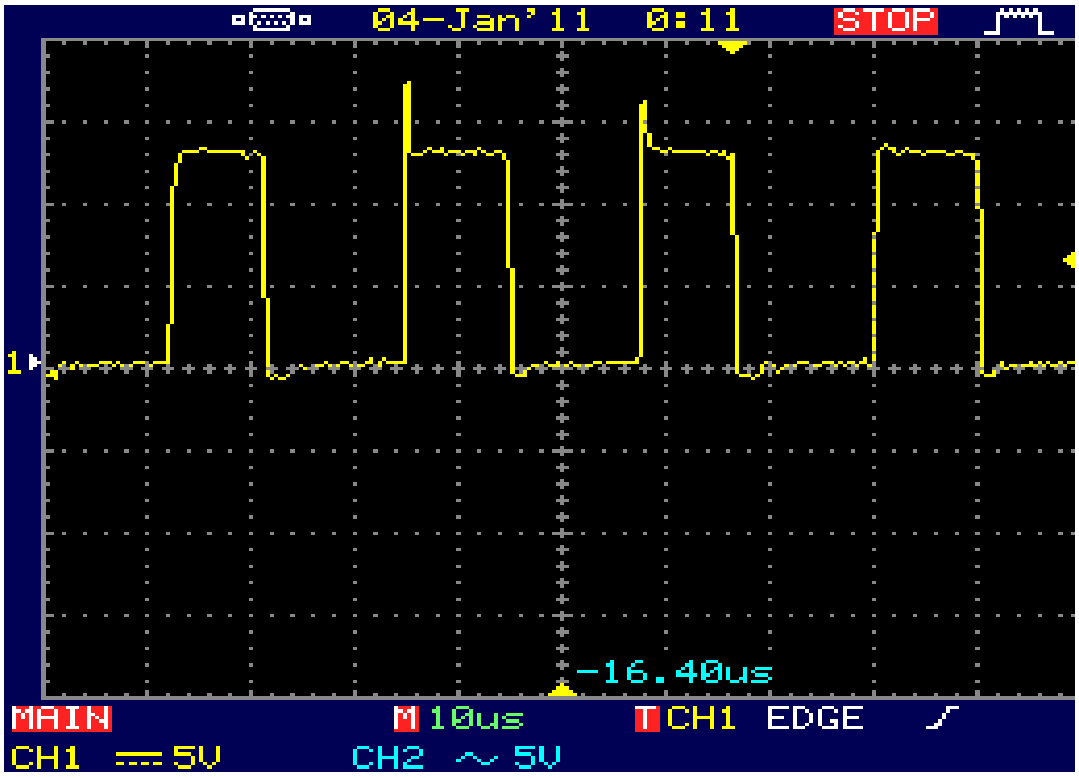

Figure 4.9: The MOSFET Voltage Stress of the Basic Boost Converter

4.4 Comparative Study about Experimental Results

By compared the result of the simple boost converter and the basic boost converter the last one increase the output voltage by 2.5 volt it’s evidently shown in figure 4.4and 4.8, moreover the voltage stress of the simple boost converter is greater than the voltage stress of the basic boost converter it’s seemingly revealed in figure 4.5 and 4.10 that mean power losses decreased according with piece of evidence the high step voltage gain can be achieved if the power losses diminish.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

DC-DC converters employ insulated gate bipolar transistors (IGBTs) and metal oxide silicon field effect transistors (MOSFETs) as they possess attractive switching capabilities, especially in terms of switching frequency and power ratings. DC- DC switching converters are becoming popular in industrial area and these converters suitable for applications where the output DC voltage needs to be larger than the DC input and can offer technical advantages economic.

This thesis has studied three Transformerless topologies with simple structures to reduce the power losses by decrease the switch voltage stress since The MATLAB simulation results for the topologies and experimental results for the basic improved structure is built in the laboratory are well in agreement with the theoretical results. Then Transformerless DC-DC Converters with high step up voltage gain can be achieved and it is appropriate solve problems invoked with interfacing the output voltage of photo-voltaic (PV) cells to grid.

5.2 Future Work

The topologies of boost converter were covered in this thesis can be enhanced to propose a novel boost converter structure with a new result to achieve high power efficiency.

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