Analysis of a Delay Compensated Deadbeat Current Controller for Inverters

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ABSTRACT

Deadbeat control is one of the most attractive control techniques, as it exhibits very fast dynamic response. Deadbeat control has been widely applied in power electronics for Pulse Width Modulation (PWM) inverter. This control technique places all the system closed-loop poles at the origin of the z-plane. Hence, it can achieve fast dynamic response with low Total Harmonic Distortion (THD), even under nonlinear loads. In existing deadbeat control techniques for single-phase UPS inverters, the pulse width of the inverter output voltage is limited by the computation time of the controlling processor. With the development of power semiconductor devices that can switch at very high speeds, feedback control techniques have been considered for inverters in UPS systems. Classical open-loop techniques of obtaining sinusoidal output voltages are incapable of providing a satisfactory response with nonlinear or fast-changing loads.

In this thesis current control of a single phase PWM inverter connected to the grid is studied. The main objectives of the control are that the current has minimum harmonic distortion and is in phase with the grid voltage. The control system should have fast dynamic response when distortion occurs and should be robust against drift in the system parameters. In this thesis delay problem of a dead beat current controller for inverter is investigated by applying the z-transform technique. A Simulink model is developed to investigate the performance of a control strategy proposed in the literature [1].

Keywords: PWM, THD, UPS, Deadbeat control.

ÖZ

Ölüvuruş denetimi, çok hızlı dinamik tepki sergileyen bir yöntem olarak en yaygın denetim teknikleri arasındadır. Ölüvuruş denetimi yaygın olarak güç elektroniğinde Darbe Genişlik Modülasyonlu (DGM) çeviriciler için uygulanmıştır. Bu denetim tekniği sistemin kapalı döngü kutuplarını z-düzleminde sıfır noktasına yerleştirir. Dolayısıyla doğrusal olmayan yükler altında bile düşük Toplam Harmonik Distorsiyon (THD) ile hızlı dinamik tepkiye ulaşılabilir. Tek fazlı kesintisiz güç kaynağı (KGK) çeviricilerde uygulanan mevcut ölüvuruş denetim tekniklerinde, çevirici çıkış geriliminin darbe genişliği kontrol işlemcisinin hesaplama süresi ile sınırlıdır. Çok yüksek hızlarda anahtarlama yapabilen güç yarıiletkenlerinin geliştirilmesi ile, KGK sistemlerindeki çeviriciler için geri beslemeli denetim tekniklerinin uygulanması gündeme gelmiştir. Sinüs çıkış gerilimi elde etmek için uygulanan klasik açık çevrim teknikleri, hızlı değişen veya doğrusal olmayan yükler ile tatmin edici bir sonuç vermekte yetersiz kalmaktadır.

Bu tez çalışmasında, şebekeye bağlı tek fazlı DGM çevirici için akım denetimi incelenecektir. Denetimin ana amaçları, akımın harmonik bozulmasını asgariye indirgemek ve şebeke voltajı ile olan faz kaymasının olmamasını sağlamaktır. Denetim sistemi yükteki oynamalar durumunda hızlı dinamik tepki vermeli ve sistem parametrelerindeki kaymalar karşısında dayanıklı olmalıdır. Bu çalışmada bir çevirici için uygulanan ölüvuruş akım denetleyicisinin gecikme sorunu z-dönüşümü tekniği kullanılarak incelenmiştir.

Anahtar Kelimeler: DGM, THD, KGK, Ölüvuruş denetim.

To my dear parents who supported me throughout my studies,

And my lovely sister (Sara) as well.

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LIST OF ABBREVIATIONS AND SYMBOLS

AC	Alternative current
A/D	Analog to digital
BJT	Bipolar junction transistor
C	Capacitor
DC	Direct current
IGBT	Insulated-gate bipolar transistor
L	Inductor
MOSFET	Metal-oxide semiconductor field-effect transistor
PWM	Pulse width modulation
THD	Total harmonic distortion
UPS	Uninterruptible power supplies
ZOH	Zero-order-hold
$i_L[k]$	The inductor current measured at the kth sampling instant
$\overline{i_L}[k]$	The local average value of the inductor current during the kth sampling period
L	The total inductance of L-C filter
R_L	The effective series resistance of filter inductors
Ts	The sampling period of A/D converters
$\overline{V_{inv}}[k]$	The local average value of inverter output voltage during the kth sampling period
$\overline{V_o}\ [k]$	The local average value of the main voltage during the kth sampling period

Chapter 1

INTRODUCTION

In this thesis current control of a single phase PWM inverter connected to the grid will be studied. The main objectives of the control are that the current has minimum harmonic distortion and is in phase with the grid voltage. The control system should have fast dynamic response when disturbances occurs and should be robust against drift in the system parameters. In this thesis the delay problem of a dead beat current controller for inverters is investigated by applying the Z-transform technique. A Simulink model is developed to investigate the performance of a control strategy proposed in the literature [1].

In literature [2], a discrete-time deadbeat control strategy is proposed that completely eliminates the computation delay problem. With this approach, the time made available to the processor is considerably greater than with existing methods. Therefore, much higher switching frequencies are possible. Literature [3], gives a synthetic survey of available Current Control Techniques of the Voltage Source inverters, in high performance applications, such as AC drives, AC Power Supplies and Active Filters, where fast response and high accuracy are needed.

1.1 Description

Deadbeat control is one of the most attractive control techniques, as it exhibits very fast dynamic response. Deadbeat control has been widely applied in power electronics for controlling Pulse Width Modulation (PWM) inverters. This control technique places all the system poles at the origin of the z-plane. Hence, it can

achieve fast dynamic response with low Total Harmonic Distortion (THD), even with nonlinear loads.

In existing deadbeat control techniques for single-phase UPS inverters, the pulse width of the inverter output voltage is limited by the computation time of the controlling processor.

With the development of power semiconductor devices that can switch at very high speeds, feedback control techniques have been considered for inverters in UPS systems. Classical open-loop techniques of obtaining sinusoidal output voltages are incapable of providing a satisfactory response with nonlinear or fast-changing loads.

Feedback control approaches for UPS inverters can be broadly classified as continuous-time and discrete-time. Continuous-time control strategies are implemented using analogue techniques and are not as reliable as discrete-time strategies.

The instantaneous feedback control technique has a reasonably fast transient response. However, this approach has the disadvantage that harmonics are generated in the output voltage at frequencies around the switching frequency.

Discrete-time control strategies are mostly based on the deadbeat control theory. Deadbeat control is one method to ensure that the output voltage or current matches to the references at the sampling instant, so adopting this control method to the utility interactive inverter, the response of the system is considerably improved with a small LC filter.

Theoretically the controlled current is forced to arrive at reference at the end of each sampling period. Many successful cases are found in shunt-type active power filters. A PWM rectifier would be the simplest case.

The input current is controlled by applying the basic deadbeat control technique to achieve unity power factor operation.

In DC/AC conversion there is now a general preference to use voltage-source rather than current-source inverters. This trend, which grew in the last two decades, is mainly justified by the introduction of power devices with self turn-off capability and by the advantages of a capacitive DC storage, over an inductive one, in terms of weight, cost and efficiency.

Chapter 2

INVERTERS

2.1 Introduction

An inverter converts a DC input into an AC output statically, that is without any rotating machines or mechanical switches. The power circuit configuration of an inverter consist of semiconductor power devices that function as static switches, that is , switches without moving contacts. The inverter also has a switching control circuit that provides the necessary pulses to turn on and turn off each static switching element with the correct timing and sequence. These switches are repetitively operated in such a way that the DC source at the input terminals of the inverter appears as AC at its output terminals, and they can be Thyristor's, IGBT's, BJT's, MOSFET's.

2.1.1 The AC Frequency

In static inverters, the Ac frequency is precisely adjustable by adjustment of the switching frequency of the power switching elements. This is determined by the frequency of a clock oscillator in the switching control section in the inverter.

2.1.2 The Magnitude of AC Voltage

The voltage may be varied by varying the DC input voltage to the inverter. In this case, the adjustment is outside the inverter and is independent of the inverter switching.

The alternative way of AC voltage variation is within the inverter by a technique called pulse width modulation (PWM).

Inverters are widely used in industrial application such as;

a) Adjustable speed AC motor drives;
b) Uninterruptible power supplies (UPS);
c) Induction heating;
d) Standby power supplies.

Static inverters may be classified into one of the following categories, on the basis of the type of AC output.

1. Voltage source inverters;
2. Current source inverters;
3. Current regulated inverters;
4. Phase controlled inverters.

Inverters can be classified into two groups according to the application area of the inverter;

1. Single phase inverters;
2. Three phase inverters.

2.2 Schematic of Inverter

Inverters can be classified in various ways. In most applications voltage fed inverters are used. The input DC voltage may be from the rectified output of an AC power supply, in which case it is called “DC link inverter”. Alternatively, the input DC may be from an independent source such as a battery.

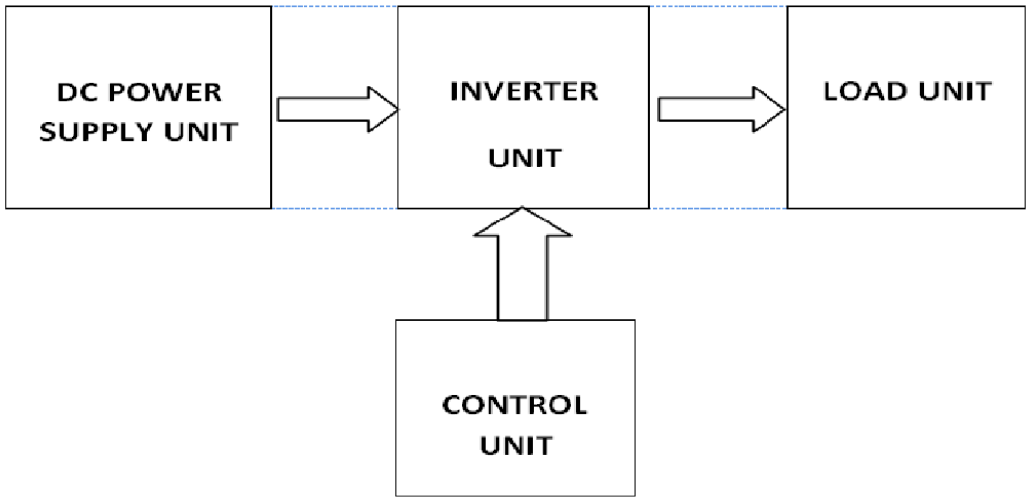

Figure 1: Control Diagram of the Inverter

2.3 Type of Inverter

There are two types of single phase bridge inverters such as;

a) Half bridge single phase inverters;

b) Full bridge single phase inverters.

2.3.1 Single Phase Half Bridge Inverter

The half bridge inverter has two controlled static switching elements, which are labeled Q1and Q2 and each of which has an anti-parallel diode. As shown in Figure 2 the input DC to the half bridge has to be a split power supply. This means that beside the positive terminal and negative terminal the mid-potential terminal, labeled 0, must be available. If the mid-potential voltage source is not available, two capacitors, labeled C1 and C2 can be connected in series across the DC source as shown in Figure 2. The load can be resistive, inductive, capacitive …etc.

To operate the inverter to provide an AC output of frequency fs, the switches Q1 and Q2 are turned on and turned off alternately, each switch being kept on for half period of the AC, while the other is kept off. It is important to ensure that both the switches are never on simultaneously at any time. If that happens, it is equivalent to a short-circuit across the DC input, resulting in excessive current and possible damage to the switching elements. For this reason it is customary in practical inverters to provide a "dead time" after the turn off of one switch and the turn on of the other. If the load is pure resistive the current and voltage will be in phase but the magnitude of the current depends on the resistance value.

Now assume a pure inductive load so the operation of the inverter will be impossible because there are no alternative paths for current. When Q1 is off the current cannot fall to zero instantly, because of inductance L, which has stored energy. So the solution for this problem is to use Diodes in parallel with switching devices. During the first half period when Q1 is on, if the current is negative Diode 2 become forward biased and turns on, and during second half period when Q2 is turned on, if the current is positive Diode1 becomes forward biased and turns on and the terminal *a* will get connected to the terminal *0* instantly.

The voltage and current waveforms of a single phase half bridge inverter for the inductive load are shown in Figure 3.

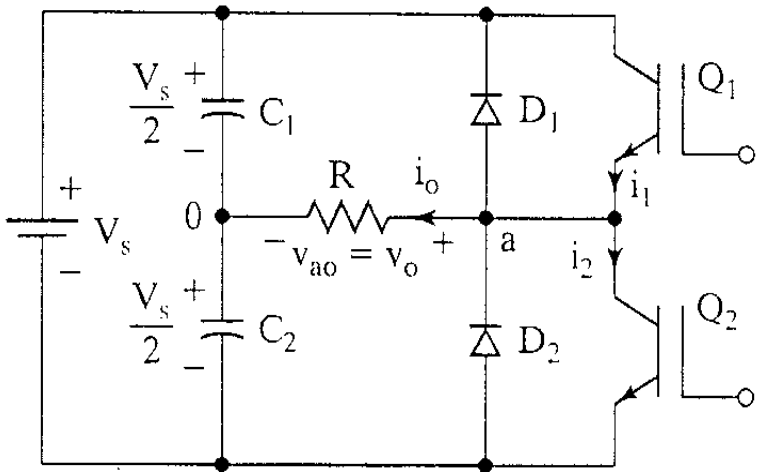

Figure 2: Single Phase Half Bridge Inverter [6]

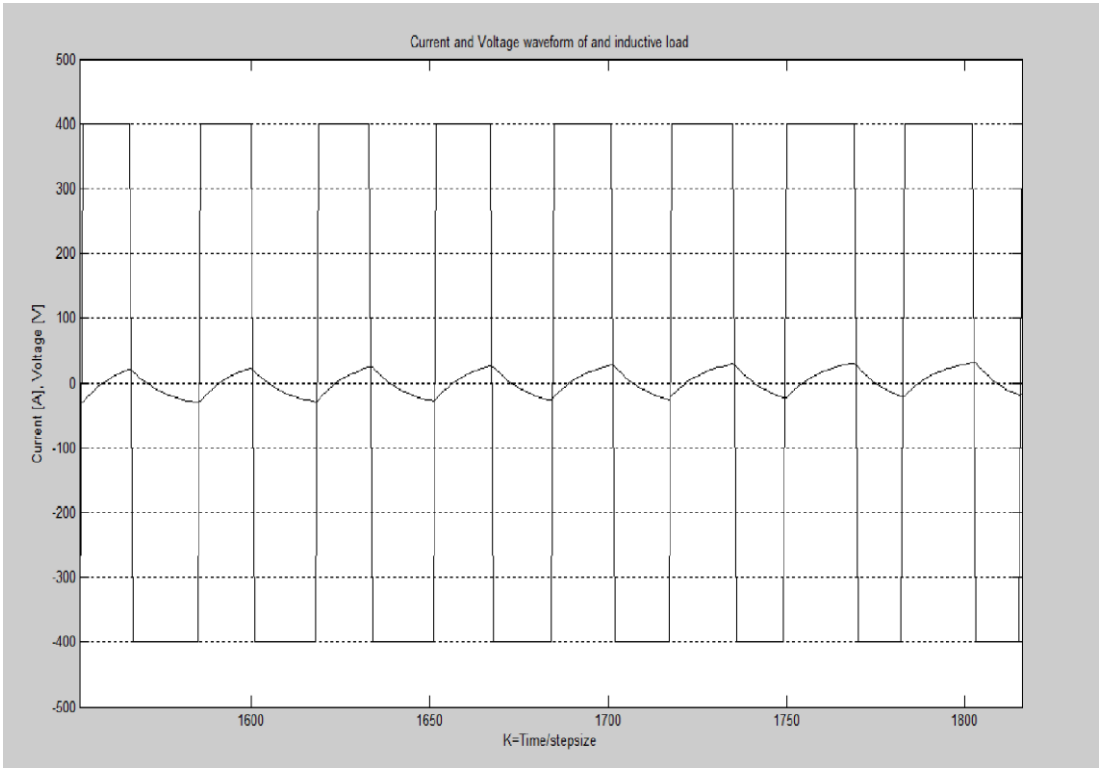

Figure 3: Voltage and Current Waveforms of an Inductive Load

2.3.2 Single Phase Full Bridge Inverter

The full bridge inverter has four switching devices each consisting of a controlled switch and its anti-parallel diode. The switches Q1 and Q2 are turned on and kept on for half period of the AC. Next Q1 and Q2 are turned off and the switches Q3 and Q4 are kept on for the duration of the negative voltage half period.

This inverter is preferred at higher power rating. The main advantage of this kind of inverter is that with the same DC input, the maximum output of the full bridge inverter is twice that of the half bridge inverter. This implies that for the same power, the output current and the switch current are one half of those of the half bridge inverter. Figure 4 shows a single phase full bridge inverter, where there are four diodes in parallel with the switching device as well.

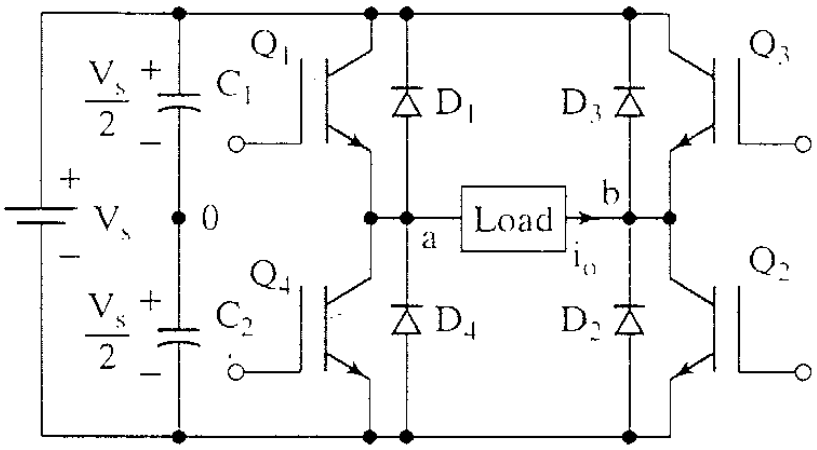

Figure 4: Single Phase Full Bridge Inverter [6]

2.4 Analysis of a Delay Compensated Deadbeat Current Controller for Inverters

Deadbeat current control is widely used in PWM DC to AC voltage source inverters for its fast response and accuracy. Based on regular sampling of load variables, the current is forced to keep up with the reference at the end of each sampling period. The circuit is connected to the mains. Although the mains voltage is assumed to be ideally sinusoidal without any need of estimation, the reference current has to be predicted by some complicated algorithm because it is rich in harmonics even in the steady state. The output current can be controlled in a deadbeat way. The deadbeat current controller suffers from a common delay in discrete systems. Nonzero computational time of the microprocessor and conversion time of A/D converters cause a significant time delay in control signal generation. The problem is severe when low speed chips are used. In this thesis the stability problem of a deadbeat current controller for inverters is first analyzed both on the z-plane and in the frequency domain.

2.5 Deadbeat Current Controller of Solar Inverters

Figure 5 shows the common power circuit of a single phase inverter. In the output there is a L-C filter. A solar inverter generally has two operation modes. In voltage mode it functions as an ideal voltage source maintaining a sinusoidal voltage waveform of fixed magnitude and frequency, like UPS. In current mode it is connected to the mains. The objective is to generate as much power as possible, so the inverter output current is controlled to operate solar panels at maximum power point. This is called maximum power point tracking (MPPT) operation.

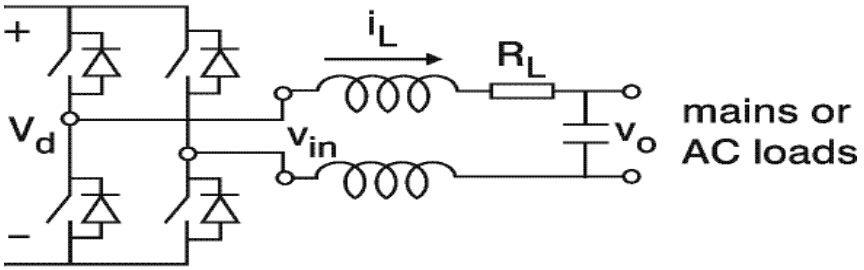

Figure 5: Single Phase Solar Inverter [1]

Assume that the capacitor current at the inverter output is negligible because the current of a 3 μF capacitor connected to the 110 V, 60 Hz mains is 0.12 A, which is only 1.3% of 9.09 A for 1 kW output power. Thus it is possible to adjust the inverter output current by controlling the inductor current. The inductor current is given by the following equation in discrete time.

$$i_L[k+1] = i_L[k] + \frac{Ts}{L}(\overline{V_{inv}}[k] - \overline{V_o} - R_L.\overline{i_L}[k]) \quad (1)$$

$iL[k]$: The inductor current measured at the kth sampling instant,

L: The total inductance of L-C filter,

Ts: The sampling period of A/D converters,

$\overline{V_{inv}}[k]$: The local average value of inverter output voltage during the kth sampling period,

$\overline{V_o}\ [k]$: The local average value of the main voltage during the kth sampling period,

$\overline{i_L}[k]$: The local average value of the inductor current during the kth sampling period.

R_L: The effective series resistance of filter inductors,

If the mains voltage is given by

$$V_o(t) = V_o \sin(\omega t) \tag{2}$$

its local average value (LAV) during the K sampling period can be estimated as

$$\widetilde{V_o} = \frac{1}{Ts} \int_{kTs}^{(k+1)Ts} V_o(t)dt$$

$$= \frac{V_o}{\omega Ts} \left[\cos(\omega kTs) - \cos(\omega(k+1)Ts\right] \tag{3}$$

Once $Ts, L, \overline{Vo}\,[k]$ are known with $R_L.i_L[k]$ being neglected. And $iL[k]$ is sampled at the Kth sampling instant, the LAV of the inverter output voltage required to regulate the output current can be synthesised from eqn. (1) by

$$\overline{V_{inv}}[k] = \frac{L}{Ts}(i_r[k+1] - i_r[k]) + \widetilde{V_o}[k]$$

$$= u[k] + \widetilde{V_o}[k] \tag{4}$$

Where $i_r[k+1]$ is the value of the reference current at the $(k+1)$th sampling instant, and $u[k]$ represents the controller output signal,

$$u[k] = \frac{L}{Ts}(i_r[k+1] - i_r[k]) \tag{5}$$

The pulse width of the inverter output voltage is easily determined by

$$D[k] = \frac{\overline{V_{inv}}[k]}{V_d} \tag{6}$$

where V_d is the DC bus voltage.

Substituting eqn. (4) into eqn. (1) it is seen that the inductor current is forced to keep up with its sinusoidal reference current at the end of each sampling period, except for the difference caused by possible estimation error of the mains and the voltage drop due to the inductor effective series resistance:

$$i_L[k+1] = i_r[k+1] + \frac{Ts}{L}(\widetilde{V_o}[k] - \overline{V_o}[k] - R_L.\overline{i_L}[k])$$

$$= i_r[k+1] + \frac{Ts}{L}\Delta V_o[k] \qquad (7)$$

The current error term $\frac{Ts}{L}\Delta V_o[k]$ determines the steady-state performance of a deadbeat controller. To reduce it the effective series resistance of the filter inductor should be made as small as possible.

2.6 Effect of a Delay of One Sampling Period

To smooth the inductor current waveform, the sampling frequency *fs* is usually chosen as high as possible. Unfortunately, a high sampling frequency implies a severe time delay in the controller. In the control block diagram in Figure 6 the switches and zero-order-hold, represent the sample-and-hold, operation. A time delay exists from sampling the inductor current to the control signal $u[k]$ generation. It is mainly composed of the computational time required for the microprocessor and the data conversion time of A/D converters. As sampling frequency becomes high, the delay time may extend to one full sampling period. In practice, the sampling period is usually chosen to be just enough to complete data sampling and control signal calculation to achieve fast response current control. The time delay induces not only inaccurate results but also an unstable system.

For simplicity, a delay of one sampling period is assumed for analysing the problem. To analyse the delay effect on the z-plane, first redraw the discrete equivalent of the mixed control block diagram in Figure 7. The delay of one sampling period is modelled by the z^{-1} block, and the ZOH equivalence of the inductor transfer function is given by

$$i_L[k+1] = i_L[k] + \frac{Ts}{L}\, u[k]$$

$$z\, I_L(z) = I_L(z) + \frac{Ts}{L}\, u(z) = I_L(z) = \frac{\frac{Ts}{L}}{z-1} u(z)$$

$$Gd(z) = \frac{Ts}{L(z-1)} \tag{8}$$

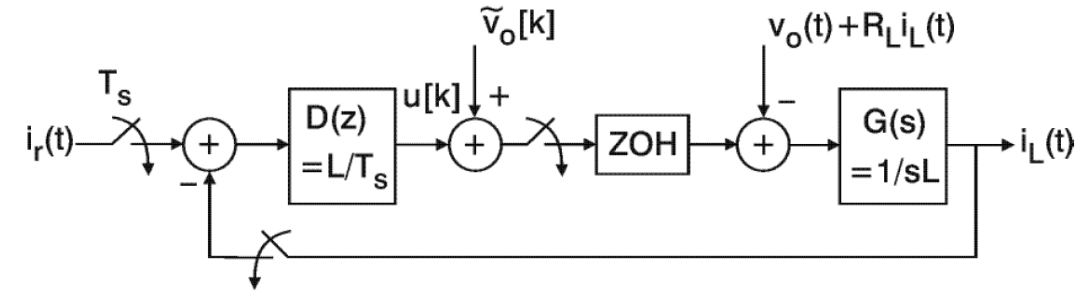

Figure 6: Block Diagram of Deadbeat Current Control Scheme [1]

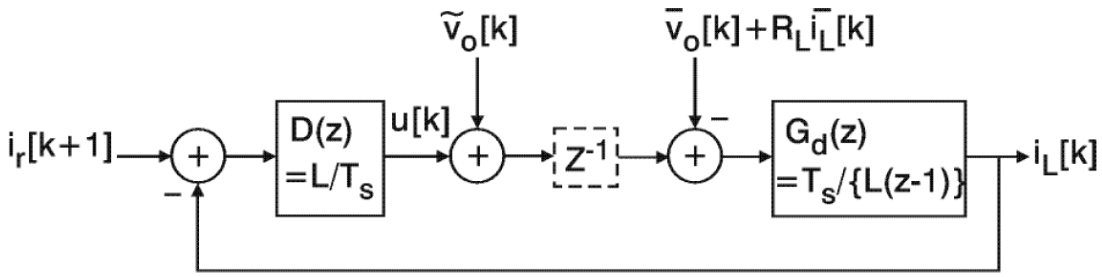

Figure 7: Discrete Equivalent of Control Block Diagram [1]

2.7 Poles of the System

2.7.1 Poles of the System without Delay

The poles of the system without delay (without the z^{-1} block in Figure 7) is easily calculated as

$$1 + D(z).Gd(z) = 0 \tag{9}$$

$$1 + \frac{L}{Ts}\frac{Ts}{L(z-1)} = 1 + \frac{1}{z-1} = 0 \quad , \qquad z = 0 \ (pole) \tag{10}$$

2.7.2 Poles of the System with Delay

However, with delay the system is found to have two problems. First the estimation of the main voltage is delayed. This can be easily corrected by supposing that the main is a sinusoidal voltage source and predicted precisely by applying eqn. (3). And the delayed control signal is difficult to compensate for.

$$1 + D(z).z^{-1}.Gd(z) = 0 \tag{11}$$

$$1 + \frac{L}{Ts}\, z^{-1} \frac{Ts}{L(z-1)} = \frac{z^2 - z + 1}{z(z-1)} = 0 \quad , \qquad z^2 - z + 1 = 0$$

$$z = \frac{1 \pm j\sqrt{3}}{2} \tag{12}$$

Compared to non-delayed system the poles are moved from origin to the unit circle.

2.8 Predictive Current Observer Based Controller

The predictive current observer is originally used in vector control of induction motors to predict rotor flux. The stator current is also predicted to avoid the computational delay in a digital controller. The observer gain can be adjusted to place system poles to be specified conjugate complex pairs in order to achieve stable control. For solar inverter application, the gain is chosen to be unity, and the inductor current in eqn. (5) is predicted during the previous sampling interval.

$$\widehat{i_L}[k] = i_L[k-1] + \frac{Ts}{L} u[k-1] \tag{13}$$

The prediction is reasonable since the control signal is generated to correct the current error. Replacing $i_L[k]$ in eqn. (5) by eqn. (13), a recursive controller equation is obtained:

$$u[k] = \frac{L}{T_s}(i_r[k+1] - \widehat{i_L}[k])$$

$$= \frac{L}{T_s}\left(i_r[k+1] - i_L[k-1] - \frac{T_s}{L} u[k-1]\right) \tag{14}$$

The control signal $u[k]$ now can be calculated one sampling period ahead. Although $\overline{Vo}[k]$ in eqn. (4) has also to be estimated one sampling period ahead, it is calculated

precisely by eqn. (3) as long as the mains is a sinusoidal voltage source. The inductor eqn. (1) is then simplified as

$$i_L[k+1] = i_L[k] + \frac{Ts}{L}u[k] + \frac{Ts}{L}\Delta V_o[k] \tag{15}$$

Apply the Z-transformation to eqn. (14) and reduce it to a non-recursive form:

$$U(z) = \frac{L}{T_s}\left[\frac{z}{1+z^{-1}}I_r(z) - \frac{z^{-1}}{1+z^{-1}}I_L(z)\right]$$

$$= \frac{L}{T_s(1+z^{-1})}[zI_r(z) - z^{-1}I_L(z)] \tag{16}$$

Apply the Z-transformation to eqn. (15) again:

$$I_L(z) = \frac{T_s}{L}\frac{1}{z-1}U(z) + \frac{T_s}{L}\frac{1}{z-1}\Delta V_o(z) \tag{17}$$

And substitute eqn. (16) into eqn. (17), the closed-loop equation is obtained:

$$I_L(z) = I_r(z) + \frac{T_s}{L}\frac{z+1}{z^2}\Delta V_o(z) \tag{18}$$

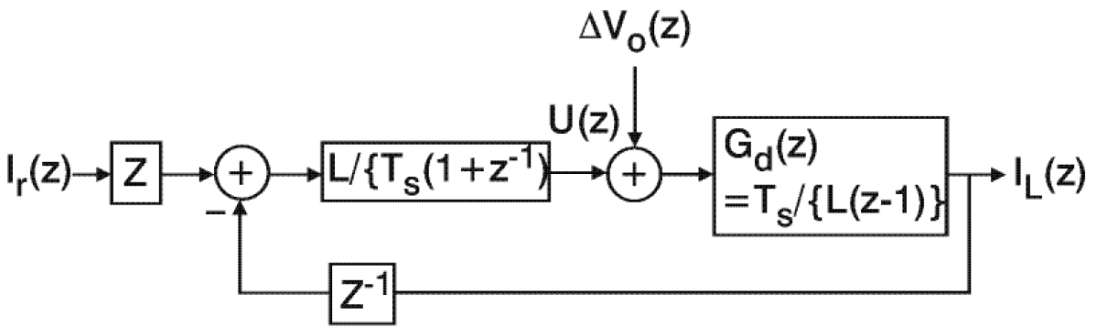

Figure 8: Control Diagram with Predictive Current Observer Based Controller [1]

If the error term on the right-hand side of eqn. (18) is neglected, a simple but precise deadbeat control results and is exactly the same as the non-delayed one. To illustrate the system stability in a similar way, the control block diagram is drawn in figure 10. The system characteristic equation is found to be

$$1 + \frac{L}{T_s(1+z^{-1})} G_d(z).z^{-1} = 1 + L(z) = 1 + \frac{1}{z^{-2}-1} = 0 \qquad (19)$$

With a double pole at *z=0.* System poles are moved back to the origin on the z-plane.

2.7.3 Poles of the System with Estimated Value of Inductance

In the previous part we studied the poles of the system with delay and without, but now we want to find out the poles of the system when the estimated value of the inductance (L_e) differs from its actual value (L). Changes in inductance will happen due to changing temperature. When such changes occur we are going to consider the sensitivity of the system when the inductance value increases. For this reason we rewrite eqn. (5) and (13) and derive our new control equation as follows.

$$u[k] = \frac{L}{T_s}(i_r[k+1] - i_L[k]) \qquad (20)$$

$$\widehat{i_L}[k] = i_L[k-1] + \frac{T_s}{L_e} u[k-1] \qquad (21)$$

$$u[k] = \frac{L_e}{T_s}(i_r[k+1] - \widehat{i_L}[k]) \qquad (22)$$

$$= \frac{L_e}{T_s}\left(i_r[k+1] - i_L[k-1] - \frac{T_s}{L_e} u[k-1]\right) \qquad (23)$$

And rewriting eqn. (31) again we can find out the new closed-loop equation;

$$i_L(z) = \frac{T_s}{L}\frac{1}{z-1} u(z) + \frac{T_s}{L}\frac{1}{z-1}\Delta V_o(z) \qquad (24)$$

$$i_L(z) = \frac{1}{z-1}\left[\frac{T_s}{L}\frac{L_e}{T_s}\,\frac{z}{1+z^{-1}}i_r(z) - \frac{z^{-1}}{1+z^{-1}}i_L(z)\right] + \frac{T_s}{L}\Delta V_o(z) \tag{25}$$

$$i_L(z) = i_r(z) + \frac{T_s}{L_e}\frac{z+1}{z^2}\Delta V_o(z) \tag{26}$$

Now we consider the characteristic equation with changing inductance;

$$1 + \frac{L_e}{Ts(1+z^{-1})}G_d(z).z^{-1} = 1 + \frac{L_e}{L}\frac{z^{-1}}{(z-1)(1+z^{-1})} \tag{27}$$

$$1 + \frac{L_e}{L}\frac{z^{-1}}{(z^2-1)} = z^2 - 1 + \frac{L_e}{L} = 0 \tag{28}$$

$$z = \pm\sqrt{1 - \frac{L_e}{L}} \tag{29}$$

If we assume that L is 30% increased $L_e = 1.3L$ the poles of the system are;

$$z = \pm\sqrt{1 - 1.3} \tag{30}$$

$$z = \pm j0.54 \tag{31}$$

As we can observe there is two complex poles and the poles moved from origin to the unity circle. Figure 9 shows the poles of the system with 30% increase in the value of inductance.

And now If assume that L is 30% decreased $L_e = 0.7L$ the poles of the system are as follows. As shown below the poles of the system has no imaginary value but it has two poles on the real axis.

$$z = \pm\sqrt{1 - 0.7} \tag{32}$$

$$z = \pm 0.54 \tag{33}$$

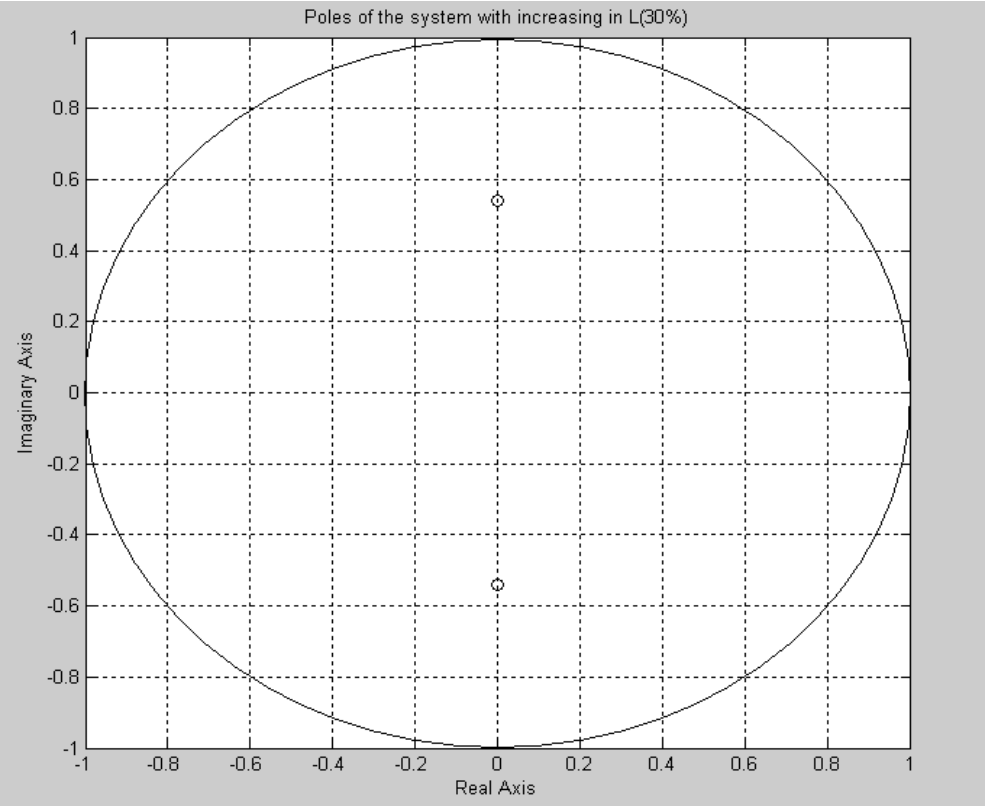

Figure 9: Poles of the System with Increasing in L (30%)

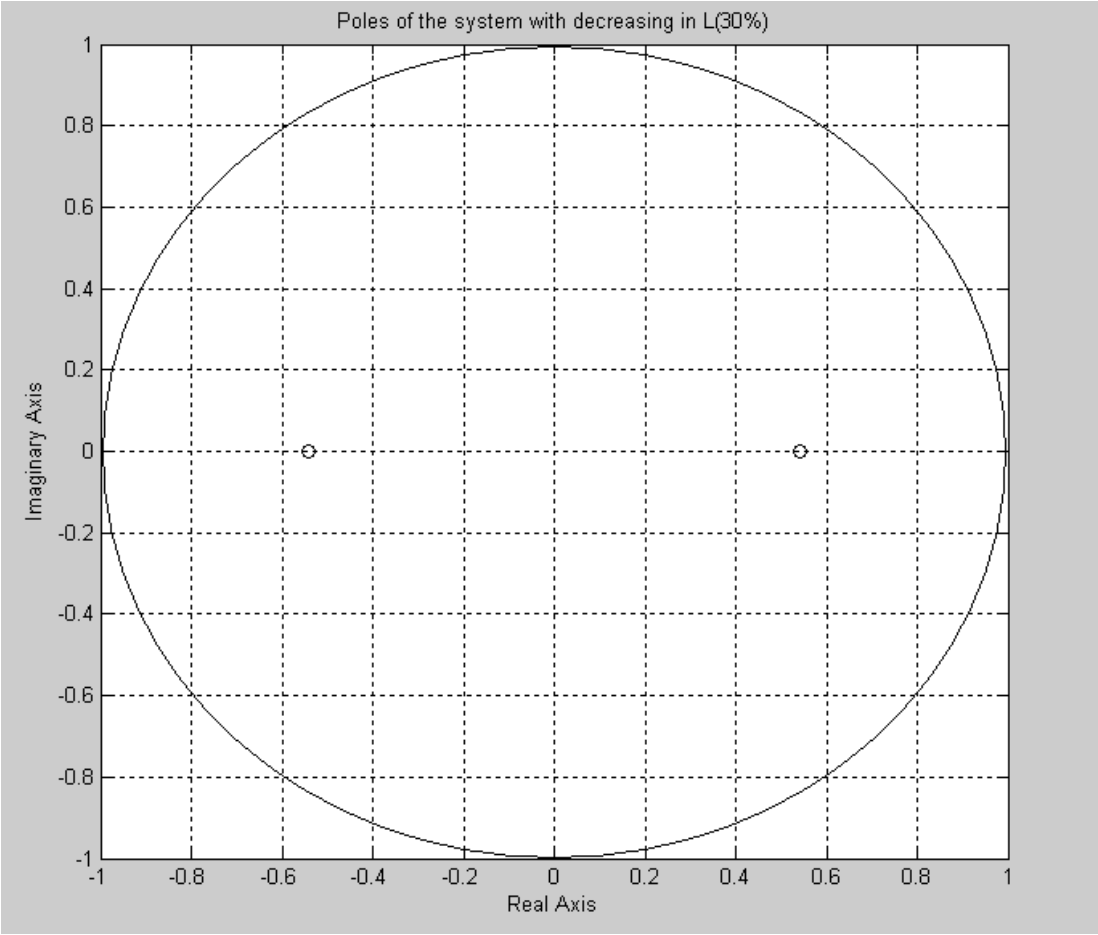

Figure 10: Poles of the System with Decreasing in L (30%)

Chapter 3

SIMULATION

3.1 Simulation of a Single Phase Inverter without Feedback

Now in simulation we used IGBT's as switching devices, and each switching device has a Diode in anti-parallel inside. So there is no need to use these Diodes out of the IGBT's. For generating pulse required to turn on and turn off the switching devices we applied the discrete PWM generator. This discrete block diagram generates pulses for carrier-based PWM, depending on the number of bridge arms selected in "generator mode" parameter. The block can be used either for single phase or three phase PWM control and the carrier frequency is 6000 Hz. We used a Demux to distribute the pulses to the IGBT's in correct sequence. The DC voltage is fixed at 400 V, and there is inductor that has a small resistor in series with it the values for inductor and resistor are 3mH and 0.1 Ω respectively.

At the output, which is our load we put a capacitor with the value of 3 μF. And also there is a main which is an AC source voltage with the value of 110 V, 60 Hz. This value is r.m.s to get peak-to-peak value we multiplied it by $\sqrt{2}$.

There are two scopes, one is for measuring the inverter output voltage while the other is for measuring the load voltage, mains voltage and inductor current. The simulation is in discrete mode in all simulation cases. Figure 11 shows the simulation model.

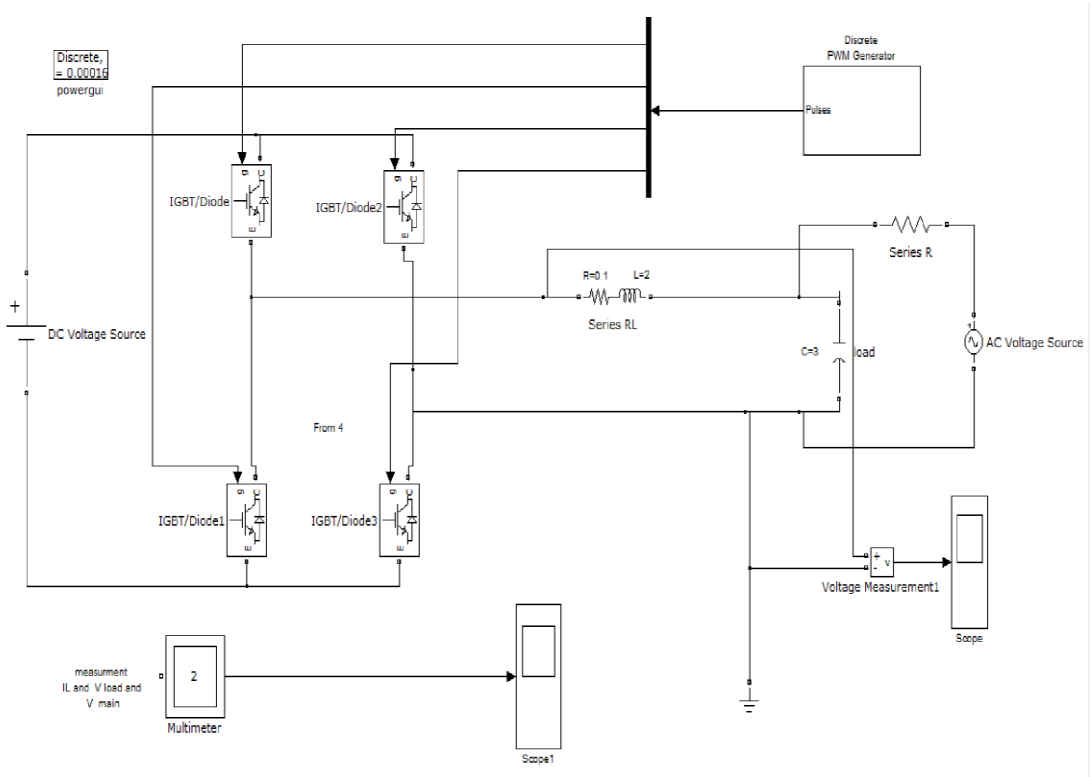

Figure 11: A Single Phase Full Bridge Inverter Connected to the Main and L-C Filter

Figure 12 shows the output voltage of the inverter which is a square waveform that represents the PWM pulses. In most of figures the x-axis represent time divided by step size that the time means our sampling time.

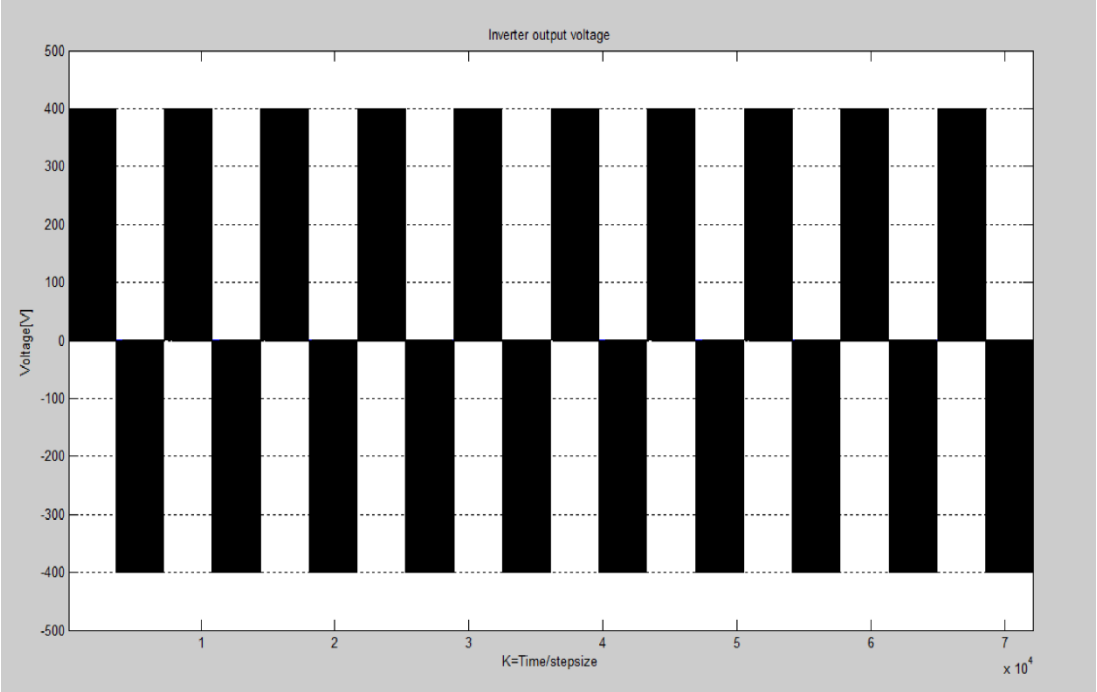

Figure 12: Inverter Output Voltage

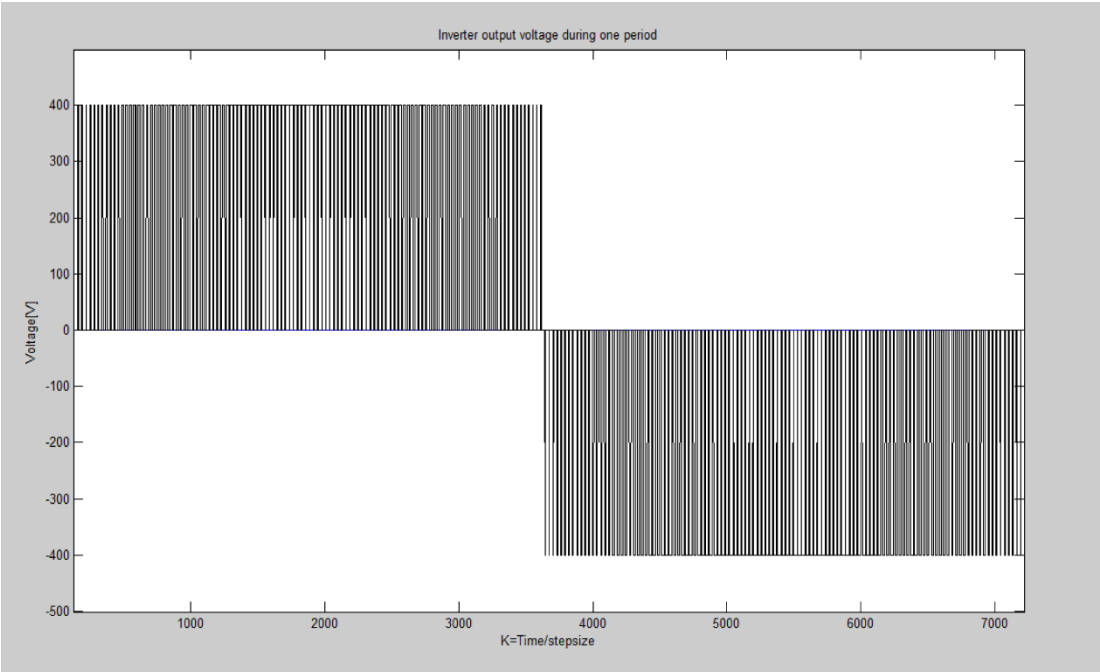

Figure 13: Inverter Output Voltage during One Period

Now Figure 14 shows the inductor current, load voltage and main voltage where the load voltage and mains voltage are approximately in phase but the amplitude of the load voltage is not the same as mains voltage and it is oscillating. And also shows the inductor current that is not in phase with the load and main voltage and it is oscillating and the amplitude is higher than load and main voltage. So our aim to improve the main and load voltage to be much more in phase and fixing the oscillation of load voltage, and to fix the inductor current to be in phase with the voltages and get rid of the oscillation of the inductor current as much as possible.

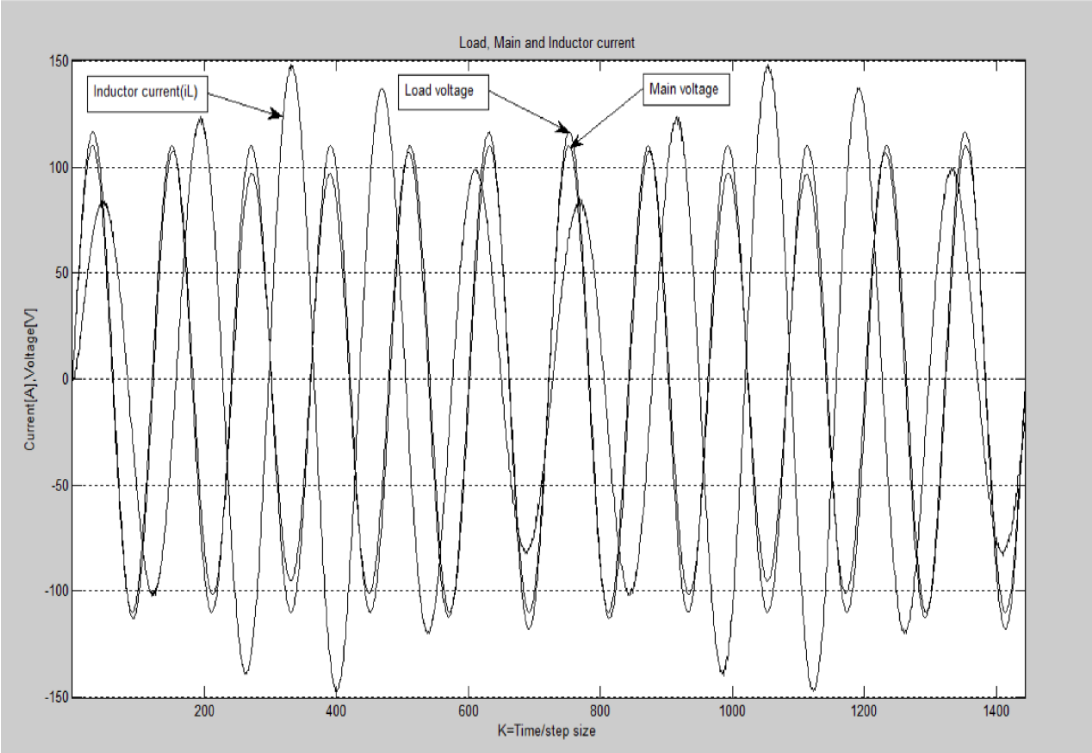

Figure 14: Load, Main, and Inductor Current

3.2 Simulation with Feedback Control

To get rid of the oscillation in inductor current we need to use feedback control. In the feedback control we measure the inductor current, so according to Figure 10 and eqn. (14) we need i_L to be advanced one sample ahead and also one sample before, so for this reason we use a sine wave as a reference current or $i_r[k+1]$ and use z^{-1} block for one sample delay as $i_L[k-1]$ and we also put a ZOH block to sample $iL[k]$ before applying z^{-1} function (ZOH) .The Zero-Order Hold block samples and holds its input for the specified sample period.

The block accepts one input and generates one output, both of which can be scalar or vector. If the input is a vector, all elements of the vector are held for the same sample period. After that we added them up and multiplied by $\frac{L}{TS}$ which is inductance value and sampling frequency this value becomes 12, so we put a Gain function and after that we needed to delay $u[k]$ by z^{-1} function and add it with previous value.

So the $u[k]$ function is ready we just needed to add this function with error term which is $\Delta Vo(z)$. It can be done by measuring output voltage which is main voltage and then add it with $u[k]$ and at the end divide it by bus voltage which is 400 V to get the pulse width of inverter output according to eqn. (6).

The aim of using rate transition is to handle transfer of data between ports operating at different rates.

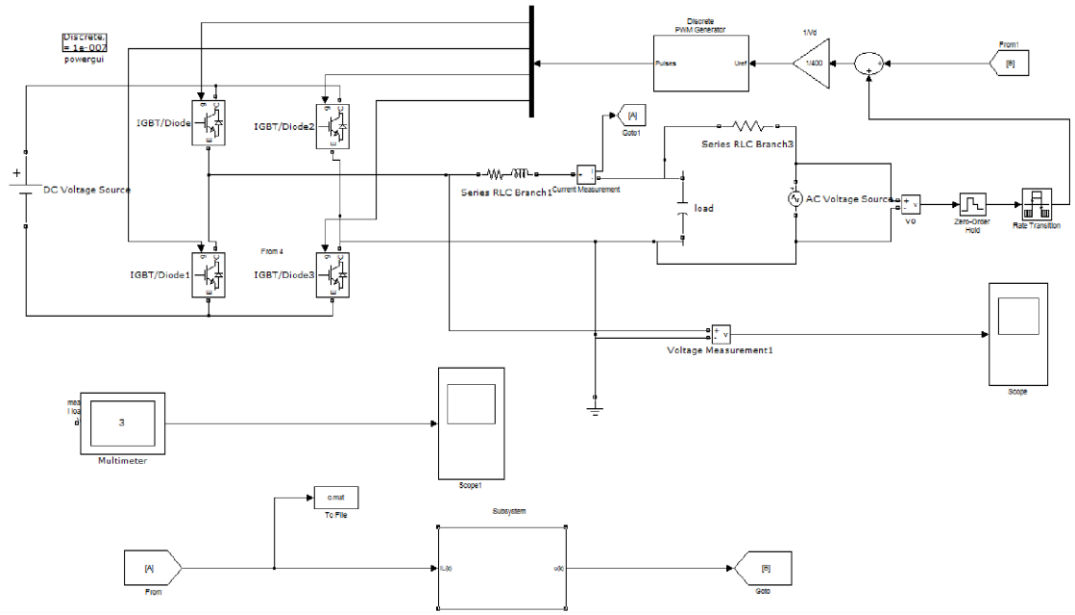

Figure 15: Shows the Circuit of a Single Phase Inverter with Feedback Block Diagram

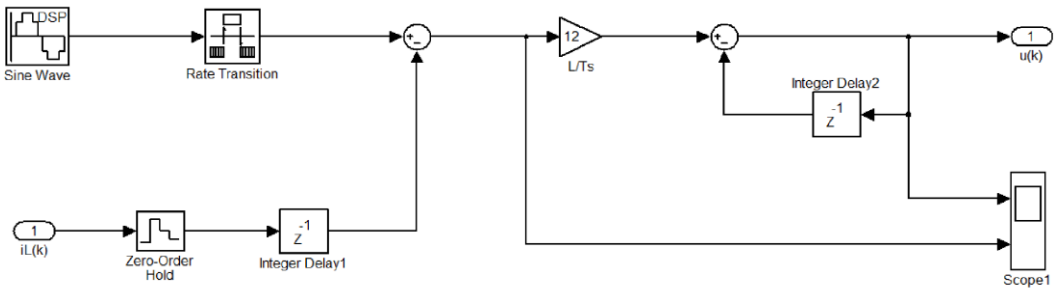

Figure 16: Shows Control Block Diagram

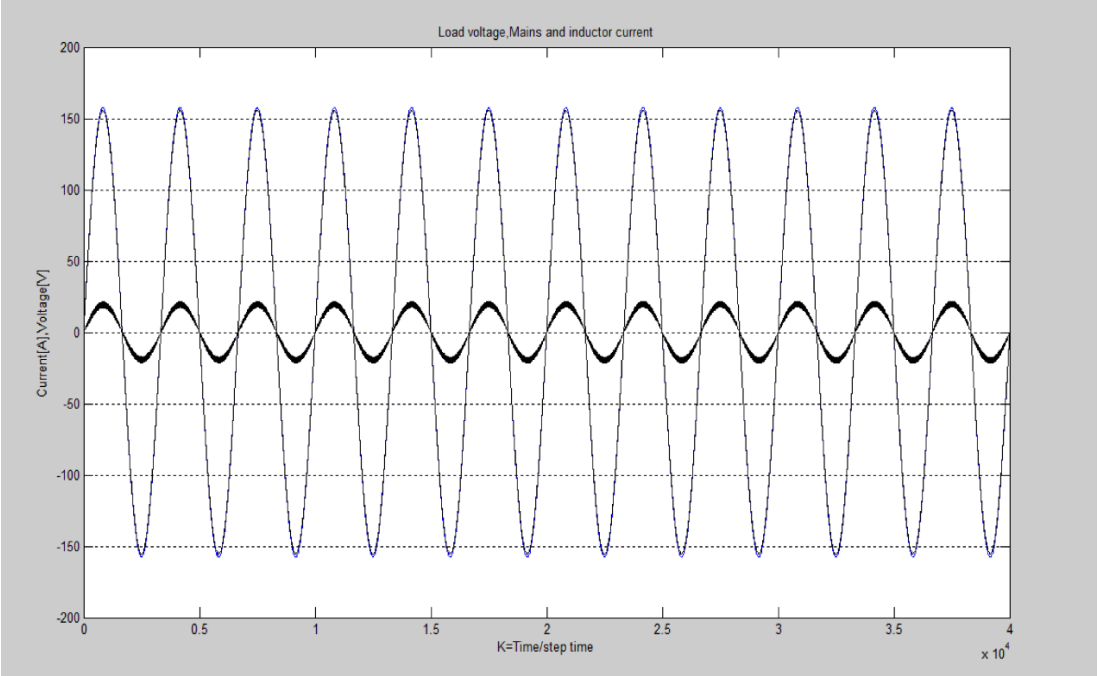

Figure 17: Load and Main Voltage and Inductor Current after Applying Feedback Control

3.3 Sensitivity of the System

3.3.1 Sensitivity of the System with Increasing the Inductance

Now we assume that the value of inductance is increasing from 5% to 30% of actual vale which is 2mH.So we need to decrease the Gain ($\frac{L}{TS}$) from 12 to 15.6.

And we calculate the THD and phase shift of the system with Fourier series.

$$iL = \sum_{n=1}^{100} an\ Sin(nwt) + bn\ Cos(nwt)$$

THD= Total harmonic distortion

$$THD = \frac{1}{I_1}\sqrt{\left(\sum_{n=1}^{100} {I_n}^2\right)} * 100\%$$

$$Phase\_shift = tan^{-1}\left(\frac{b_n}{a_n}\right)$$

As you can see in Figure 18 if we increase the value of $(\frac{L}{TS})$ the phase-shift becomes positive and small and at exact vale 15.335 it is as close as to zero it was around (0.0017).

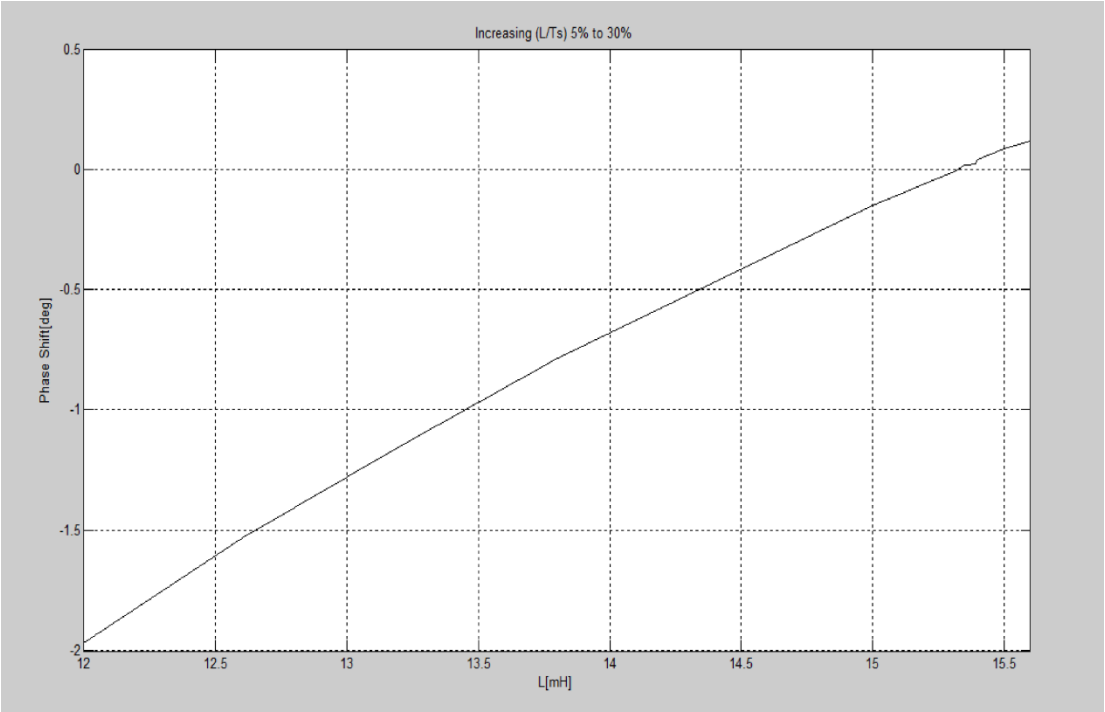

Figure 18: Increasing (L/Ts) and Phase-Shift

3.3.2 Sensitivity of the System to Inaccurate Value of Inductance

Now we decrease the value of $(\frac{L}{TS})$ from -5% to -30% of its actual value and it becomes from 12 to 9.6. It is shown in Figure 19 that if we decrease L, the phase-shift increases and it is negative at all points. So it implies that if we decrease the $(\frac{L}{TS})$ the phase-shift becomes high and negative but if we increase the $(\frac{L}{TS})$ we can

improve the phase-shift and it becomes positive and at the value of 15.335 we can have minimum phase-shift which is (0.0017).

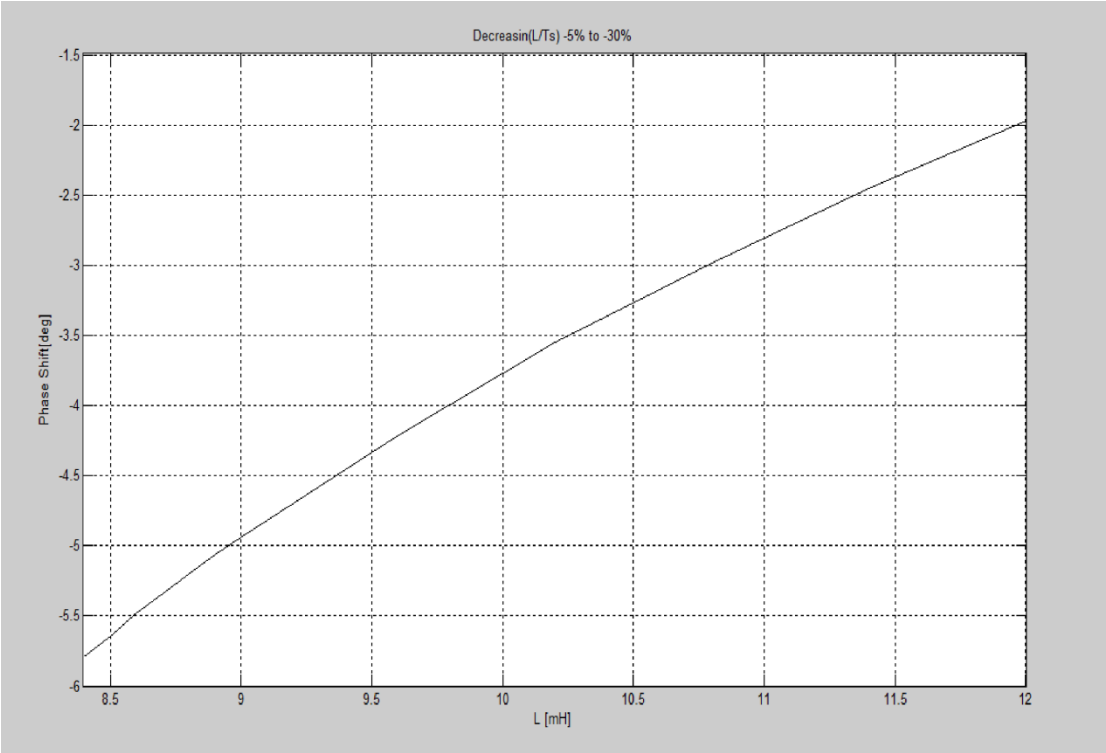

Figure 19: Decreasing (L/Ts) and Phase-Shift

3.3.3 Sensitivity of the System to the Sampling Frequency (fs)

At this point we want to show the changing in phase-shift and THD if the sampling frequency changes. Also we consider the harmonics for lower sampling frequency which is 1000 Hz and higher sampling frequency which is 12000 Hz. Figure 20 shows the phase-shifts when the sampling frequency is changed from lower to higher

values. Figure 21 shows the THD if sampling frequency changes from its lower value to higher value.

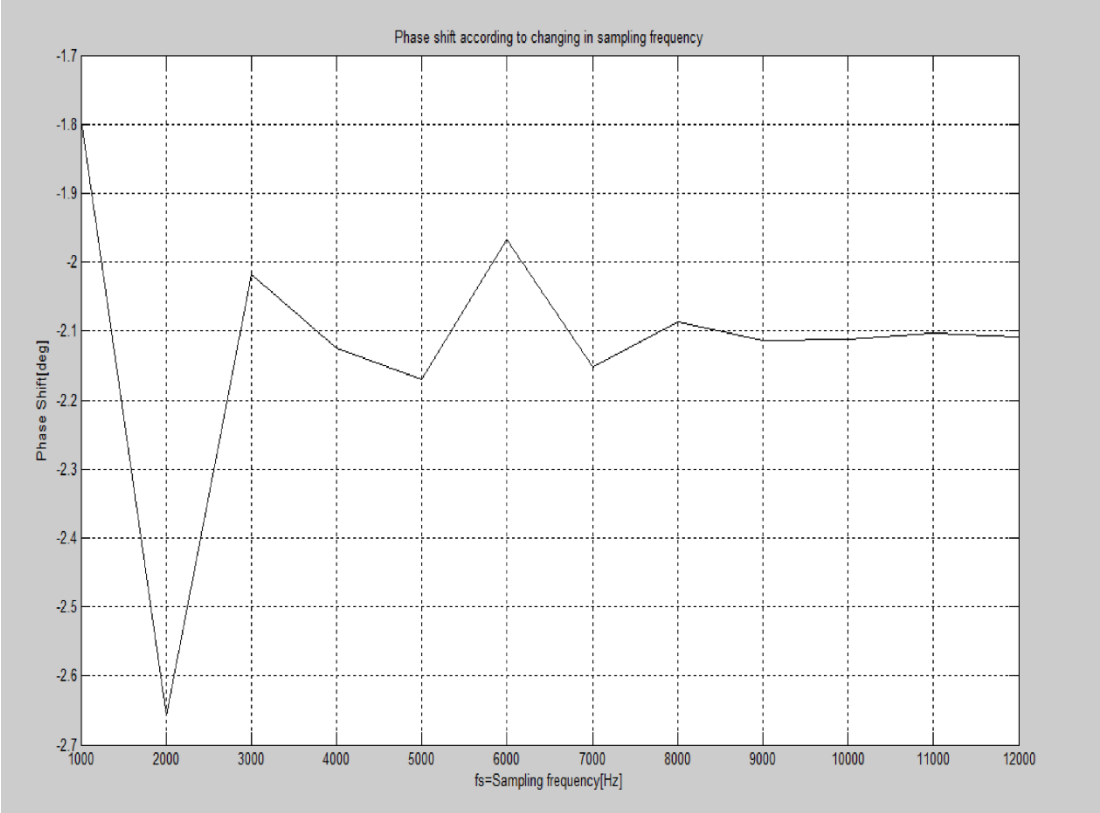

Figure 20: Phase-Shift According to Changing in Sampling Frequency

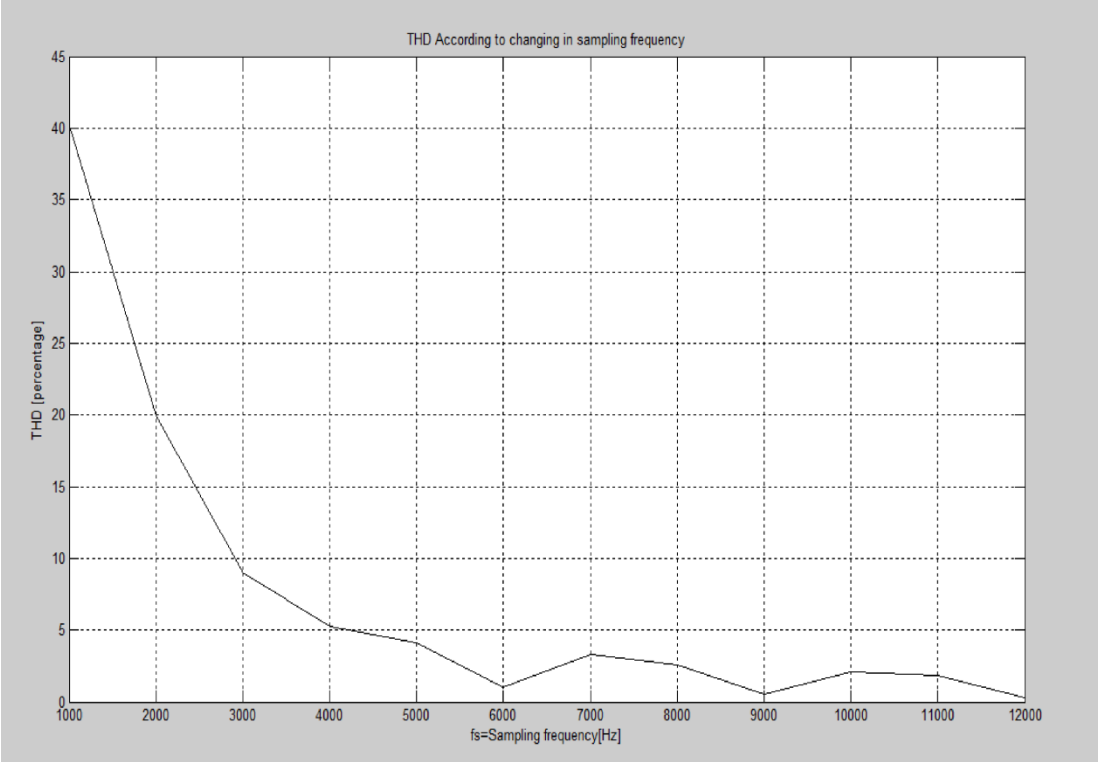

Figure 21: THD According to Changing in Sampling Frequency

Figure 22 shows the harmonics of the current at actual sampling frequency which is 6000 Hz and Figure 23 and Figure 24 shows lower sampling frequency and higher sampling frequency which are 1000 Hz and 12000 Hz respectively. So that implies that at high sampling frequency we have less harmonics and in low sampling frequency we have more harmonics. The high amplitude harmonic is the fundamental and the others are harmonics.

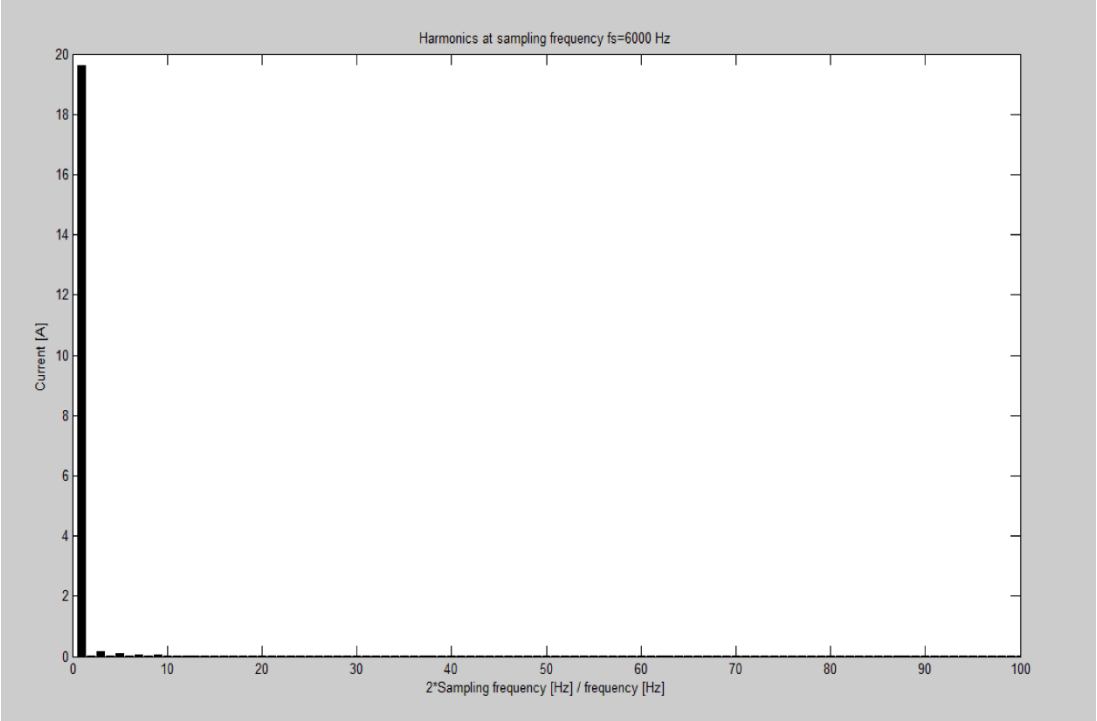

Figure 22: Harmonics at Sampling Frequency 6000 Hz

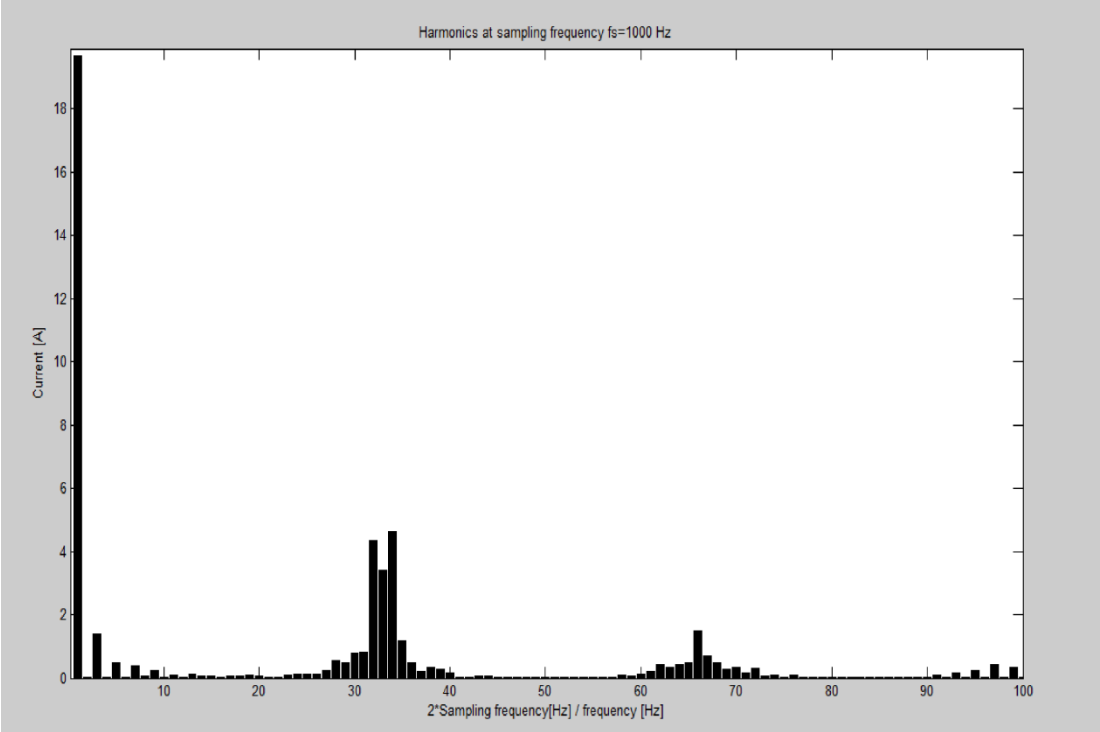

Figure 23: Harmonics at Sampling Frequency 1000 Hz

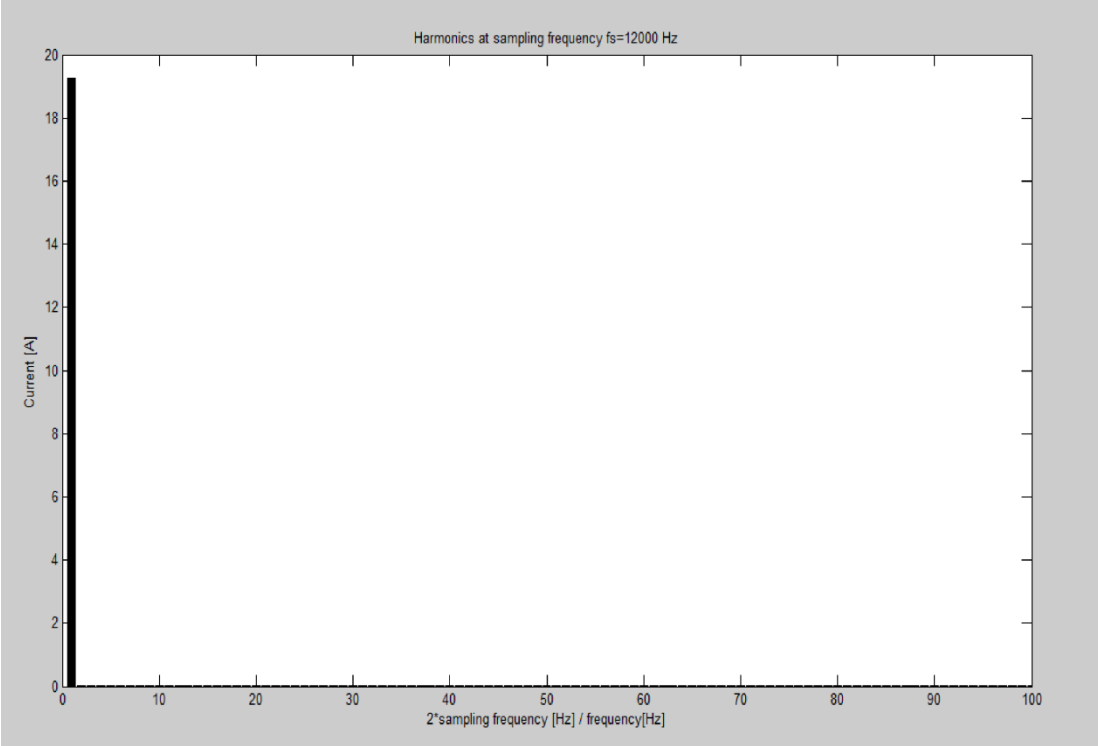

Figure 24: Harmonics at Sampling Frequency 12000 Hz

Chapter 4

STEP RESPONSE

4.1 Simulation Using Step Function in Control Block Diagram

In this part we add a new sine wave as a current reference and multiplying a step function with one step value and a gain value of 5. The aim of using step function is to see how the system responses to a step change in the references. In other words the dynamic response of the control system to the step change is investigated.

The Step block provides a step between two definable levels at a specified time. If the simulation time is less than the Step time parameter value, the block's output is the Initial value parameter value. For simulation time greater than or equal to the Step time, the output is the Final value parameter value.

We set the step function time at a specific time of t=0.75sec as seen in Figure 26. Also the new control block diagram is shown is Figure 25 and the main circuit is the same as previous in Figure 15.

The time from previous step to new step is around 7msec.The amplitude of sine wave is 15 A and new sine wave is 5 A.

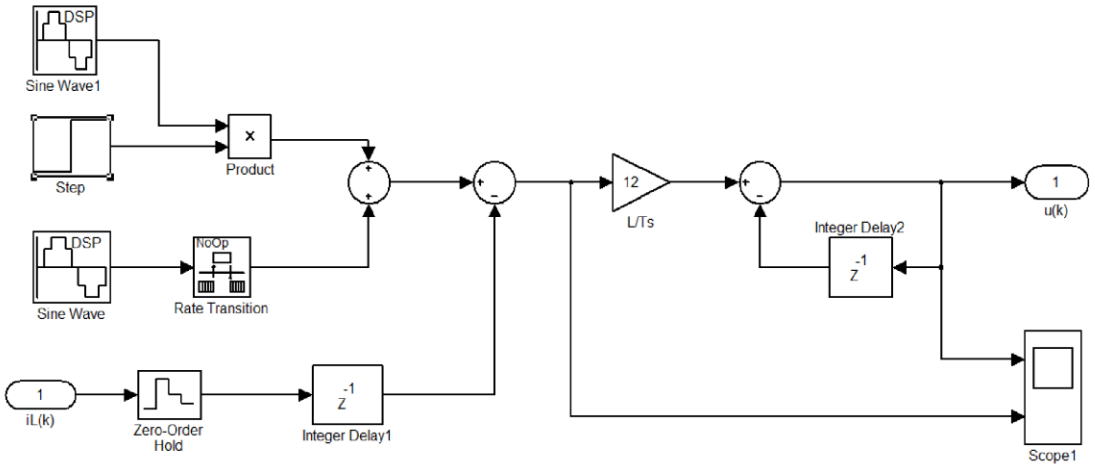

Figure 25: Control Block Diagram with Step Function

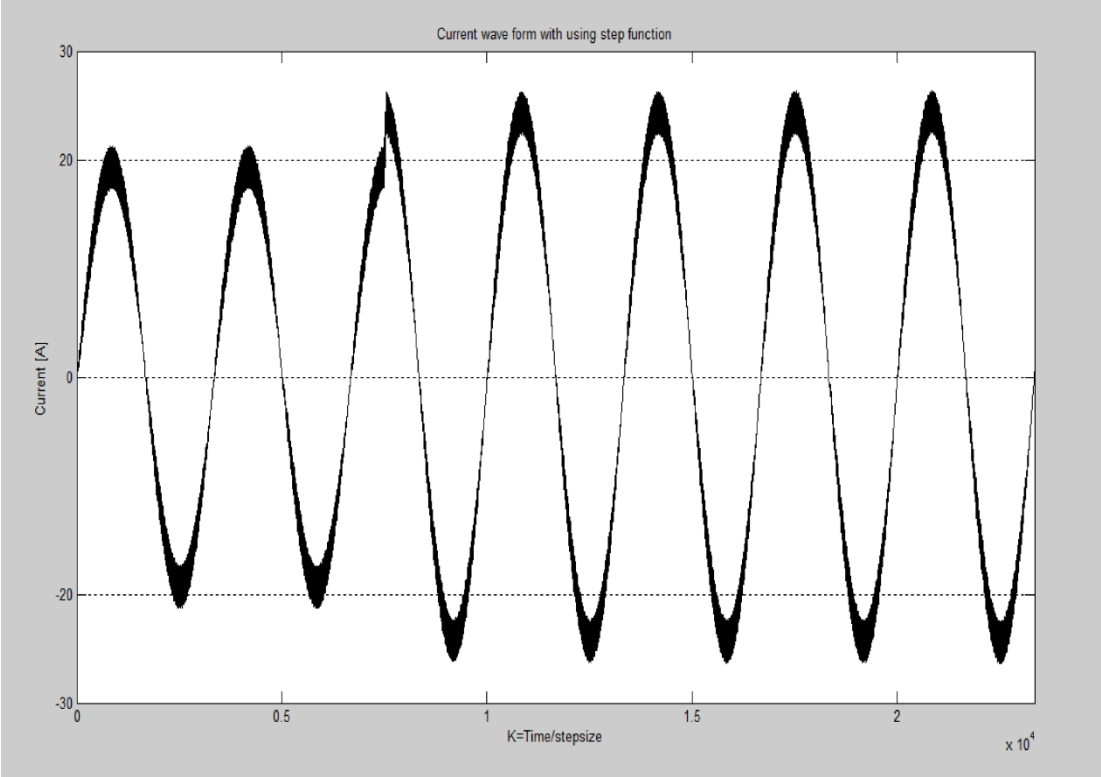

Figure 26: Current Waveform with Using Step Function

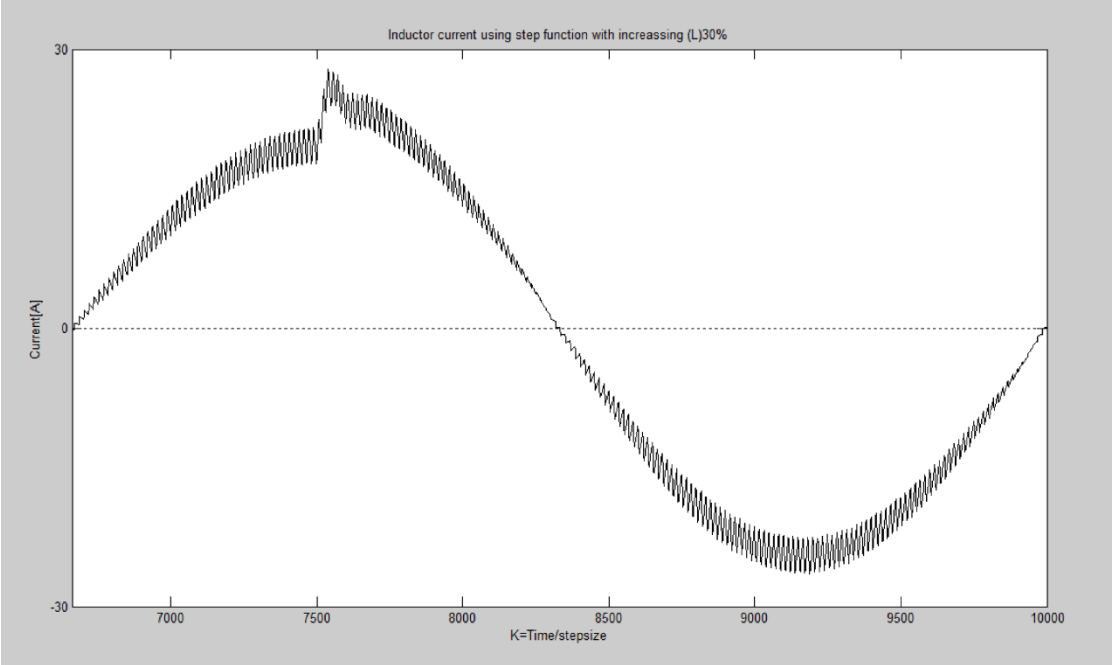

Figure 27: Inductor Current Using Step Function with Increasing L (30%)

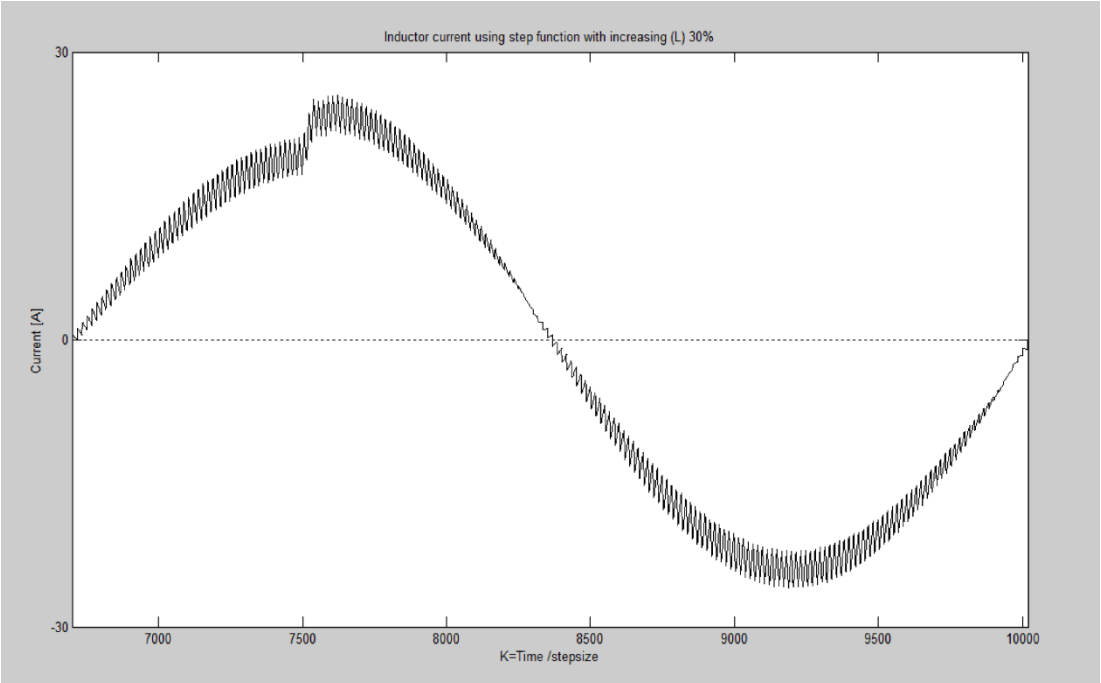

Figure 28: Inductor Current Using Step Function with Decreasing L (30%)

4.2 Creating Reference Current by Output Voltage

Now we are going to create reference current for control block, as we discussed before we created reference current by using a sine wave block, but now we want to measure the output voltage, Vo and create the reference current. But after it is done there was a phase shift between current and voltage so we use a filter which is a capacitor and a resistor in series with it, after that we measure the resistor voltage and generate the reference current from it. So first we should calculate the resistor voltage according to Figure 29 as follows

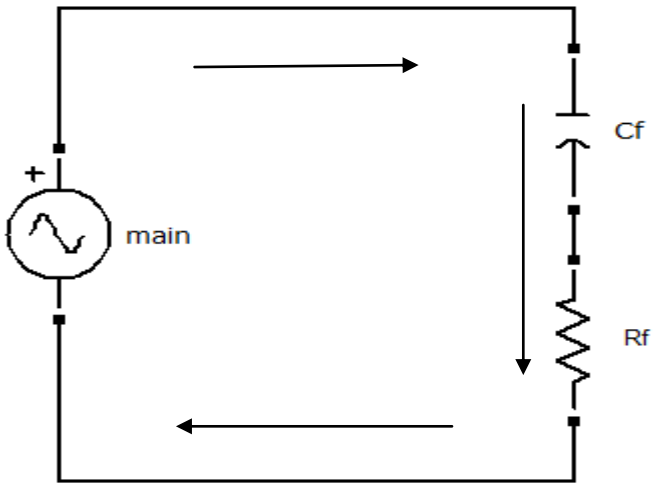

Figure 29: Output Voltage and R-L Filter

$$V_R = \frac{R}{R - jX_c} V_o = \frac{1}{1 - j\frac{X_c}{R}} V_o = \frac{1 + j\frac{X_c}{R}}{1 + \left(\frac{X_c}{R}\right)^2} V_o \qquad (34)$$

$$|V_R| = \frac{\sqrt{1+\left(\frac{X_c}{R}\right)^2}}{1+\left(\frac{X_c}{R}\right)^2}\,|V_o| \qquad \Phi = tan^{-1}\left(\frac{X_c}{R}\right) = tan^{-1}\left(\frac{1}{\omega RC}\right) = \omega Ts$$

$$= \frac{f}{fs} \quad , \quad \frac{1}{\omega RC} = tan\left(\frac{\omega 60}{6000}\right) = 0.0628 \qquad CR = \frac{1}{0.0628\omega} \qquad (35)$$

If we assume that, $R = 10k\Omega, \quad C = 4.21\mu F$

Then after writing the KVL equation we figured out the value for capacitor by assuming the value of $R = 10k\Omega$, then adding them to the circuit and measuring the resistance voltage and get a feedback to our control block. The new circuit is shown in Figure 30, and also the block diagram in Figure 31. The main, load voltage and inductor current waveform are shown in Figure 32 as well.

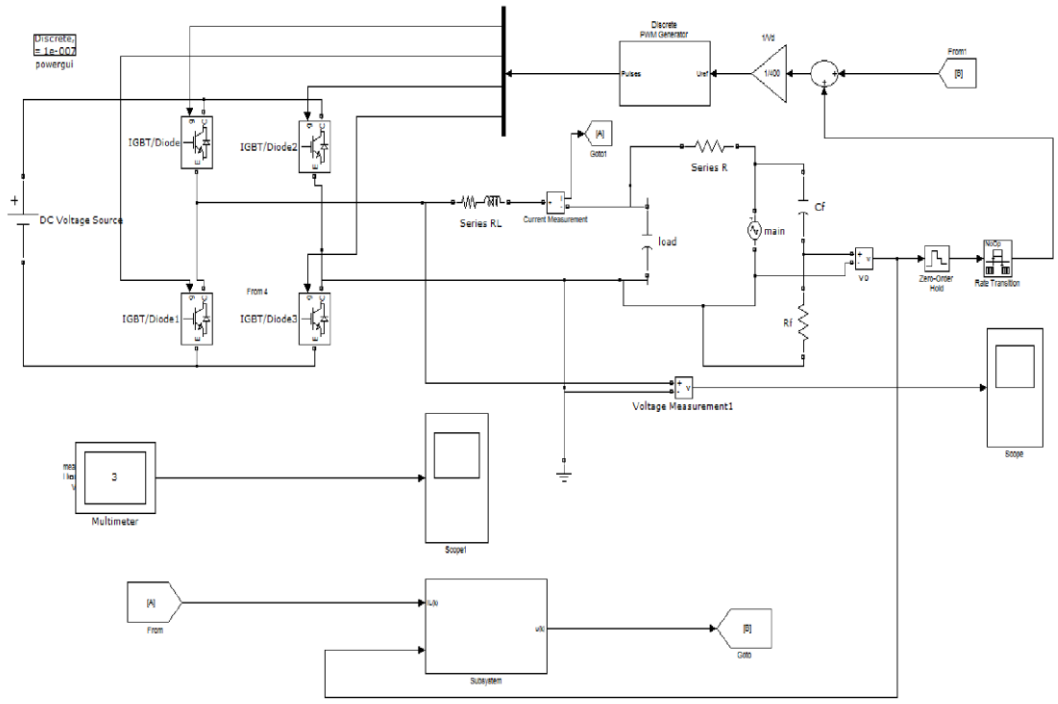

Figure 30: Single Phase Inverter Using Output Voltage as a Reference Current

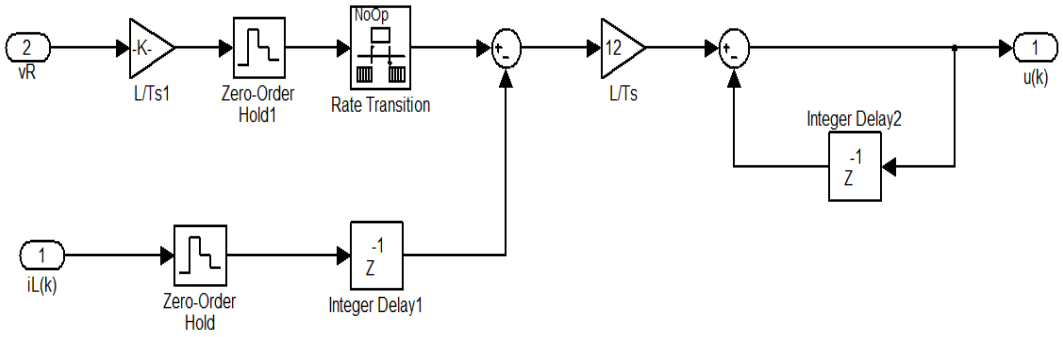

Figure 31: Control Block Diagram of Figure 26

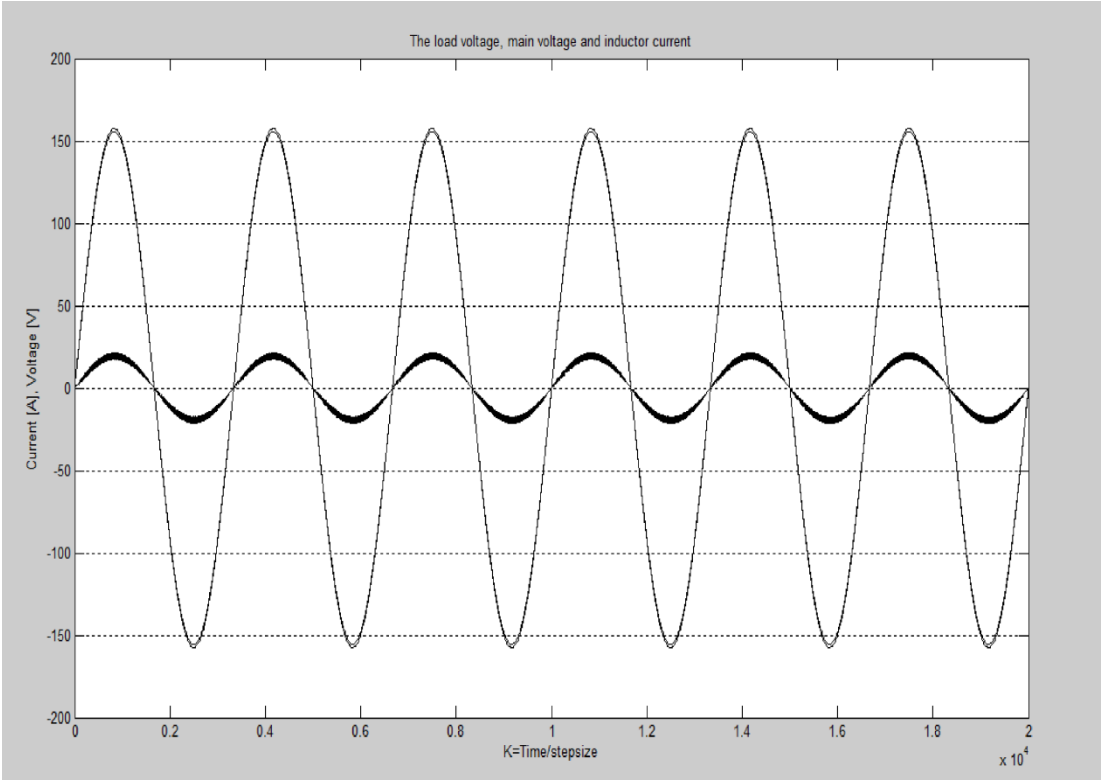

Figure 32: The Load, Main Voltage and Inductor Current Waveform

4.3 Creating Reference current by Using Output Voltage and Applying Controlled Voltage Source

In this stage we are going to create the reference current by using output voltage but as we showed in Figure 33 the source voltage is a controlled source voltage that we want to make some distortion to the output voltage and observe the inductor current due to this distortion the output voltage is of the form

$$V_o(t) = V_1 sin\omega t + V_3 sin3\omega t \qquad (36)$$

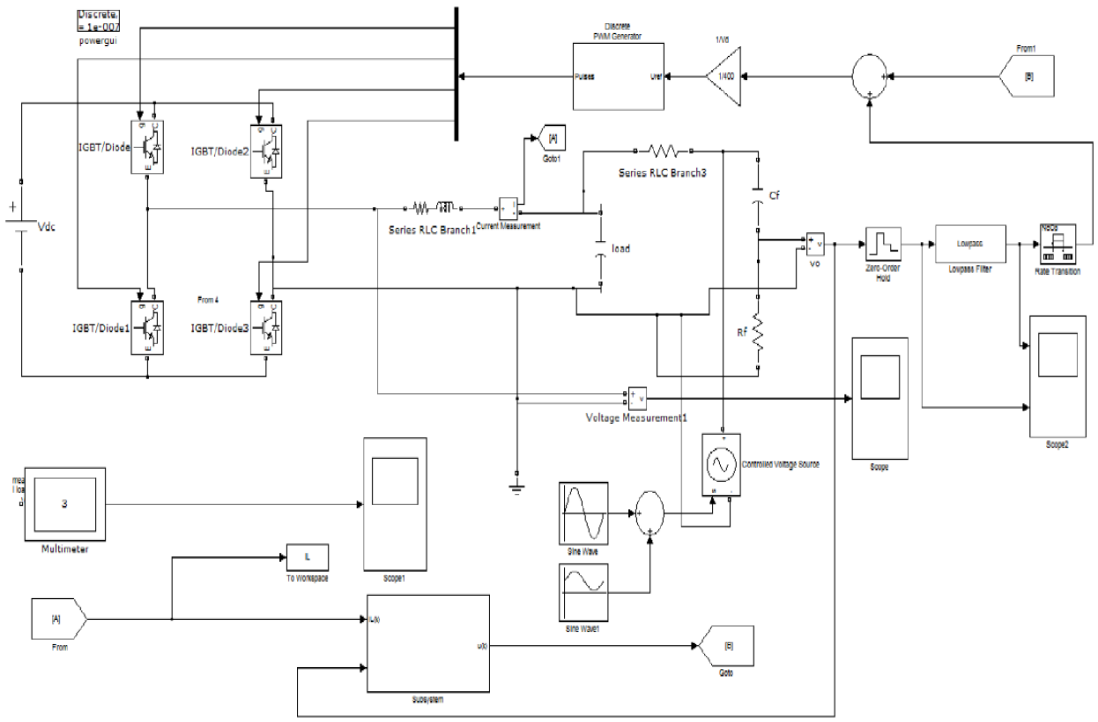

Figure 33: Creating Reference Current Using Output Voltage by Applying Controlled Voltage Source

In Figure 34 the waveform of the output voltage, load voltage and inductor current is shown. We created the non-sinusoidal output voltage and connected it to the load and then to get rid of the harmonics and phase shift we used a R-C filter and passed the measured output voltage signal through a low-pass filter block. As shown in Figure 34 there is no phase shift between the voltage and current and no distortion in output current.

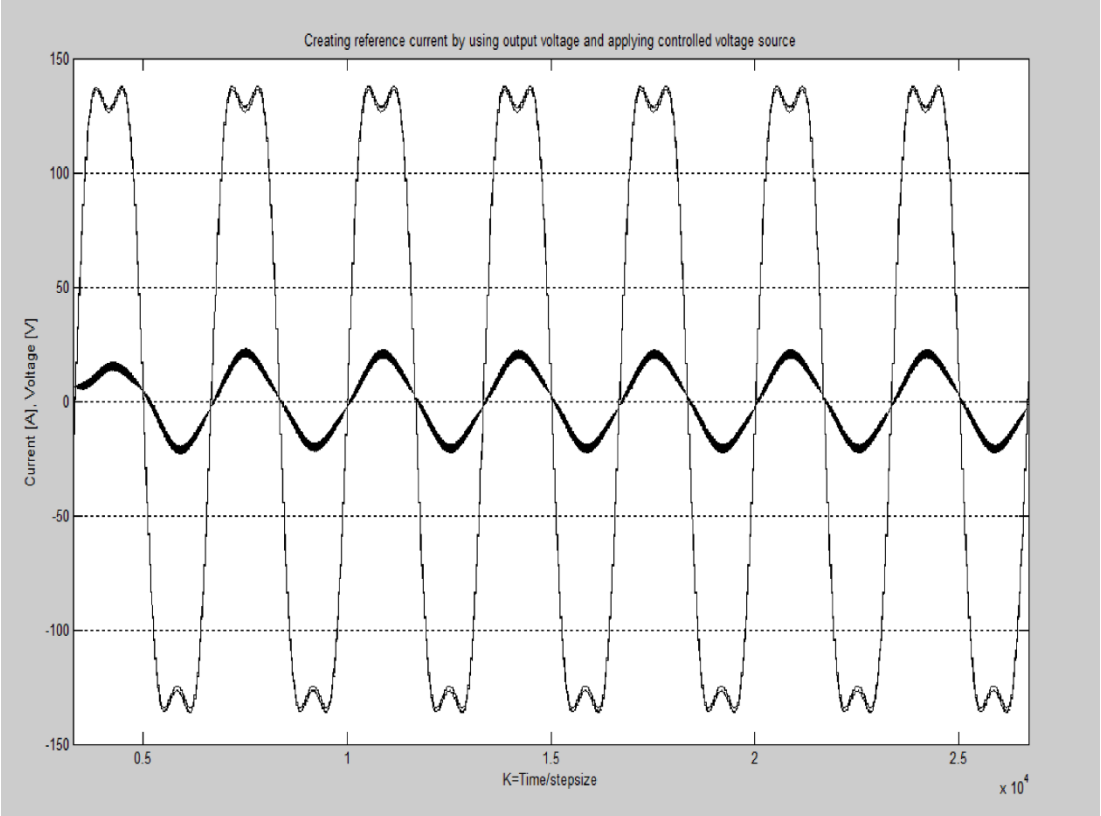

Figure 34: Creating Reference Current by Using Output Voltage and Applying Controlled Voltage Source

4.4 Comparing Phase-Shift when Reference Current Is Made from Output Voltage with Sine wave Block

We compared the two modes, when the reference current is created by a sine wave block with a reference current created by using output voltage and we considered the phase-shift between them. At actual value which is $(\frac{L}{TS})$ =12 this mode has less phase-shift. But in other parts it is different. The phase-shift is shown in Figure 35 when the reference current is output voltage and when the $(\frac{L}{TS})$ changes from its actual value from 5% to 30% increasing.

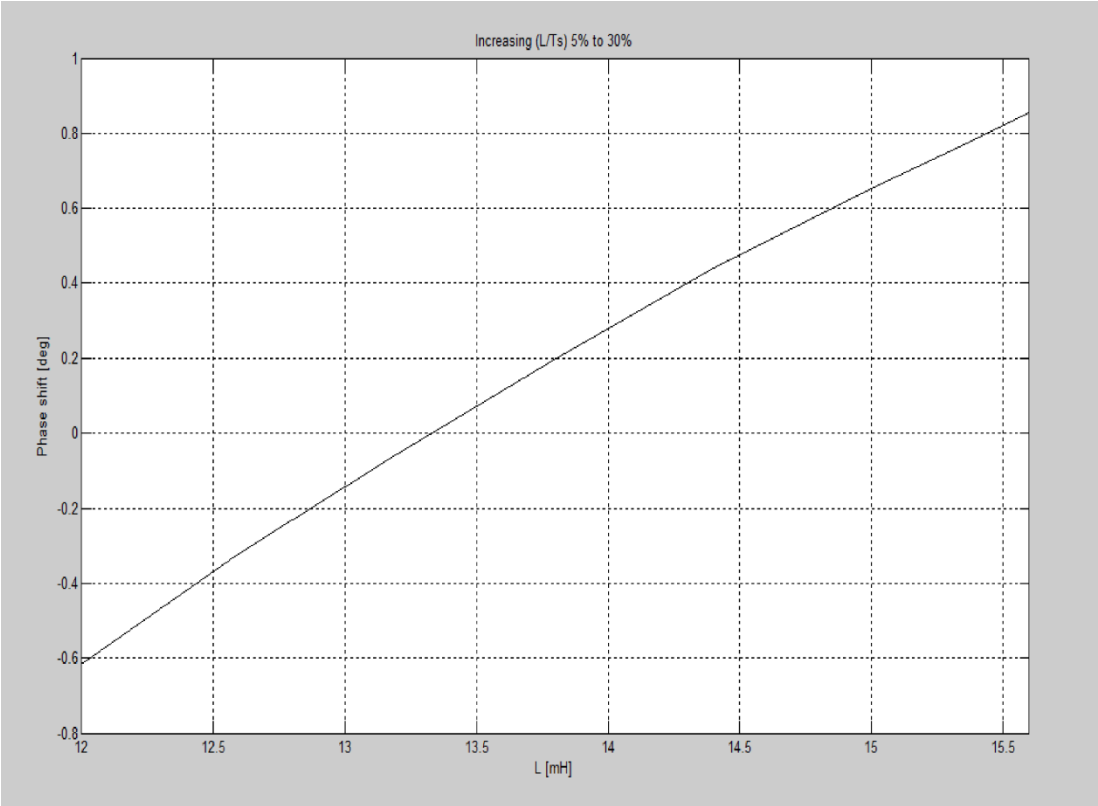

Figure 35: Phase-Shift by Changing (L/Ts) From 5%-30% Increasing

Also the phase-shift is shown in Figure 36, when $(\frac{L}{TS})$ changes from its actual value from -5% to -30% decreasing

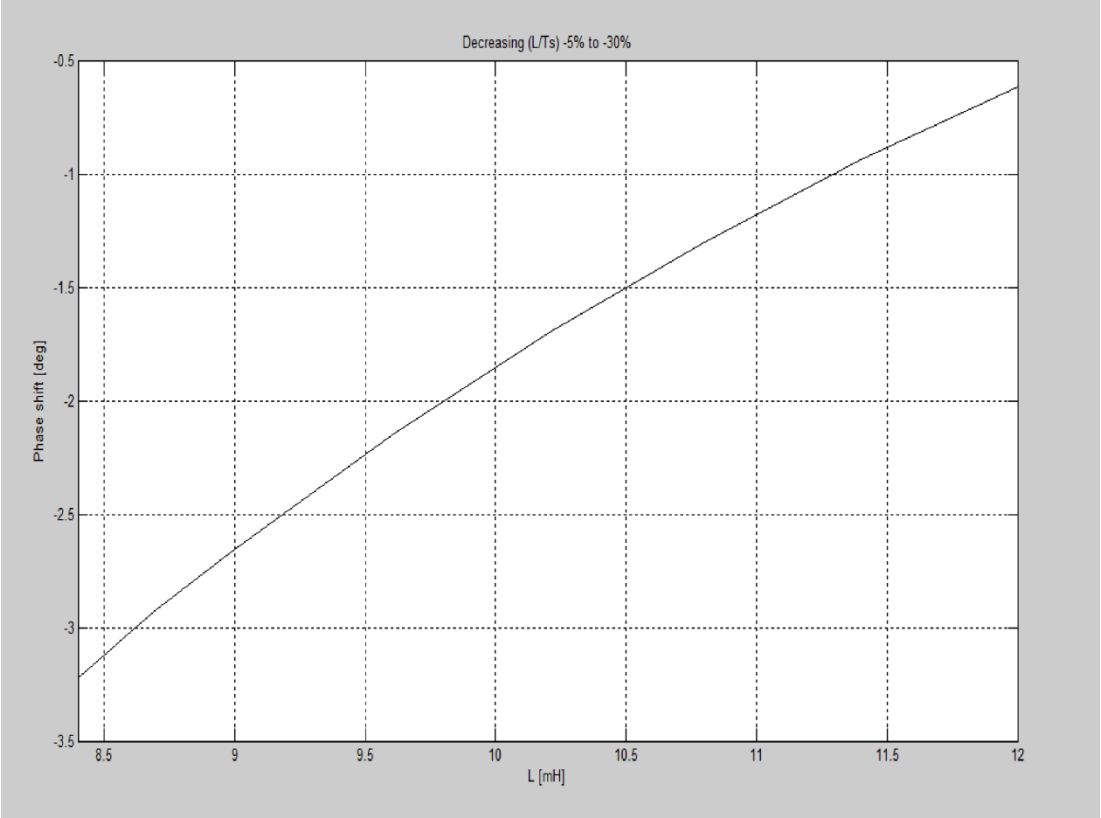

Figure 36: Phase-Shift by Changing (L/Ts) from -5% to -30% Decreasing

Chapter 5

CONCLUSION AND FUTER WORK

5.1 CONCLUSION

Time delay always exists in a digital controlled system due to the nonzero computational time of the microprocessor and conversion of A/D converters. When a low speed microprocessor is used, the delay may extend to full sampling period, which results in not only inaccuracy but also unstable current control. For solar inverter application, the analysis based on z-transform and frequency responses of system loop gain reveals that system poles are moved outward to locations on the unit circle on z-plane. In this thesis the delay problem of a deadbeat current controller for inverter is investigated by applying z-transform.

As we discussed in section 2.6 first we analyzed the effect of delay during one sampling period and then we analyzed predictive current observer based controller. In chapter 3 section 3.2 we simulated the system in MATLAB program.

We studied the sensitivity of the system by changing the inductance value in 3.3. We also applied a step function to simulation part to see the dynamic response of the system due to applying the new reference current in chapter 4, section 4.1.

And at the end we created the reference current by using the output voltage instead of using sine wave block and analyzed both type in section 4.2, and applying controlled voltage source to make distortion to output voltage in section 4.3.

5.2 Future Work

My intention for future work is mainly to implement the system in real time and using the logic elements and see the results by using microcontroller, IGBT's, signal generator. In this part the system will be implemented in time domain while in simulation the system was implemented in frequency domain and it was discrete.

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